DESIGNING AN ADVANCED PACKAGING SYSTEM FOR INFRARED SCENE PROJECTORS

by

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A thesis submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Computer Engineering

Spring 2017

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ACKNOWLEDGEMENTS

I would like to thank several people for helping me reach this point. Without their support and patience, I would not have made it this far. I would like to acknowledge my family for all of their help; as their support and wisdom has helped to keep me anchored. They have helped guide me since the very beginning, pushing me to devote myself to my studies and to learn anything and everything that I can.

My advisor, Dr. Fouad Kiamilev, has been an excellent source of inspiration and direction for this project. Without the opportunity to join the CVORG team, I would not be where I am today.

I would especially like to thank my brother, Joshua Marks, for initially proposing the idea of graduate school to me. He challenged me to grow and learn past the standard class regimes, and for that, I am deeply grateful.

I would also like to thank Andrea Waite, Rodney McGee, Jonathan Dickason, Garrett Ejzak, Casey Campbell, Jeffrey Volz, Benjamin Steenkamer, and everyone else in CVORG that has helped me succeed in so many ways here.

To everyone, thank you.

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ABSTRACT

Over the past several years, our research group has created the world's first infrared scene projector (IRSP) that uses infrared light emitting diodes (IRLEDs). This allows for the creation of higher brightness, resolution and framerate projectors to be used for infrared testing purposes. The new projectors are able to use larger hybrids containing more IRLEDs than ever before. However, adding more IRLEDs creates a heating issue. Each IRLED will create a set amount of heat by itself and even more when placed in an array with hundreds of thousands of other LEDs. The heat is generated by inefficiencies in the IRLEDs and compounded by the low thermal conductivity between the IRLEDs and the cold finger of the pour filled Dewar currently housing the IRLED array and flip-chip bonded Complimentary-Metal-Oxide-Semiconductor (CMOS) Read-In-Integrated-Circuit (RIIC).

This heating issue led to the need for a new way of cooling the hybrid down to cryogenic temperatures by the use of a Dewar chamber. The chambers that are currently available on the market were no longer sufficient, creating the need for a custom redesign. This paper focuses on the thermal management problems created by the newest IRSPs and their resolutions through a custom Dewar chamber design and subsequent fabrication.

Chapter 1

INTRODUCTION

1.1 Background

In many applications, light is often the chosen medium for communication or data collection. One of the most common forms of light that is used takes place in the infrared (IR) portion of the light spectrum. This portion of the light spectrum is advantageous in many areas, from consumer electronics to astronomy and many items in between.

For many applications, infrared devices are often used in guidance systems, such as in astronomy. It is much easier to track a heat source as it glows brightly against the relatively cool background of the sky, such as in stars. There are a few ways in which to test these devices, however, the most efficient way of doing so is through an infrared scene projector (IRSP).

The most prolific type of IRSP that is available on the market today are resistor type arrays. These take advantage of the Micro Electro Mechanical Systems (MEMS) technology. They use an array of resistors that are heated up quickly to create images that a guidance system can see. There are many limitations of this type of scene projector, which include low frame rates, being incapable of separating apparent temperature from actual thermal temperature, and the inability to emulate a non-black body spectrum.

The inherent limitations of the existing systems have created a need for a new system type, one that succeeds where the current models failed. The resultant technology that was designed was called super-latticed light emitting diodes (SLEDs). This new technology used an array of light emitting diodes (LEDs) instead of a resistor array. By doing so, this solved many of the problems of the previous types of IRSPs. As such,

SLEDs technology allowed for a higher level of accuracy in image projection while having a higher resolution [1, 2], a much higher framerate, and the eventual use of two colors in the display.

In 2014, a joint team between Dr. Fouad Kiamilev's team, CVORG, at the University of Delaware, and Dr. Thomas Boggess' team at the University of Iowa, constructed the world's first infrared light emitting diode (IRLED) projector, shown in figure 1.1. Currently, the SLEDS system is being used to understand how the IRSP technology works and how it will progress.

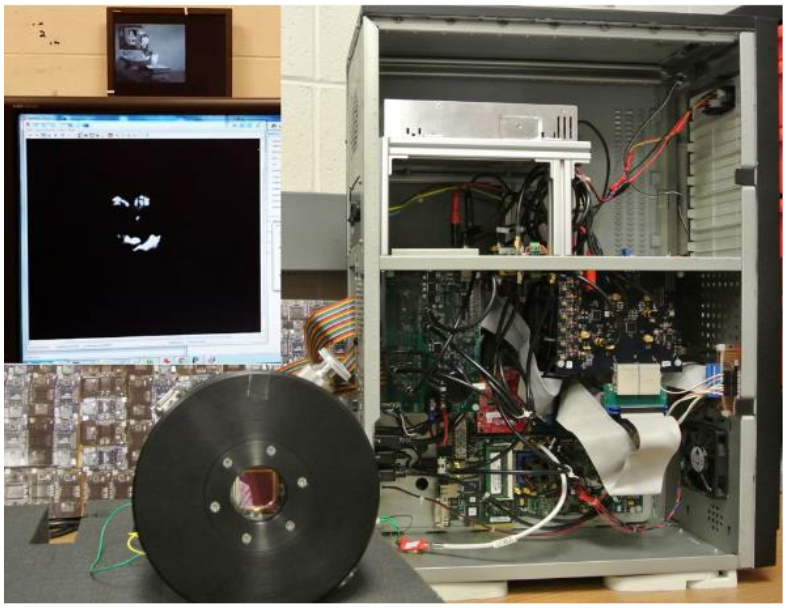

Figure 1.1: The early SLEDs system with Donald Duck in "Der Fuehrer's Face" (1943 Disney Pictures and RKO Radio), playing on the monitor

1.2 Motivation

The joint team of the University of Delaware and the University of Iowa are currently working on the next generation of the SLEDs scene projector, which is made of several versions. These versions include the Two-Color SLEDs array (TCSA), Nightglow SLEDs (NSLEDs), and High Definition Infrared Light Emitting Diode (HDILED). These newer

versions focus on improving the current system limitations, such as improved background drawing, higher framerates, and increased resolution. The current version of the IRSP is operating at a 512x512 resolution and a 100 Hz framerate [3] while TCSA is operating at a resolution 512x512 pixels with 2 SLEDs per pixel at nearly a 1 kHz framerate.

Each variation of the system, TCSA, NSLEDS, and HDILEDS, all seek to improve a key weakness of the original system. For example, TCSA seeks to be able to display two different signal strengths, or "colors" on the screen. This is advantageous as it becomes easier to differentiate the active objects, such as a target, versus the less active objects, such as the ground or sky. Additionally, newer generations of the SLEDs projector will include more and more advanced features. Currently, there are several features in mind that are being worked on by the team, such as a modular firmware that can provide a higher resolution and faster framerate as hardware channels increase [4], a real-time non-uniformity correction (NUC), and the ability to scale the packaging to accommodate any size testing unit. The work described in this paper will demonstrate how the test unit packaging was a limitation and the steps taken to overcome that obstacle.

Chapter 2

THE CURRENT SYSTEM

2.1 Small Scale Example

It is important to understand the system as both the individual components and the sum of those components. However, as the system is currently very large, a small-scale example of a 3 x 3 set of LEDs would be more useful. This example will start with the read-in integrated circuit (RIIC), the SLEDs, and the main LED driver.

Currently, the SLEDs array is made of 512 x 512 pixels with each pixel being an IRLED. An IRLED works in the same manner as a regular LED, they get brighter as the input voltage is increased. The concept of the 3 x 3 is used throughout the array and will work for any sized array.

Every pixel is in an array with both an x address and a y address that correspond to the position on the array. This can be seen in figure 2.1.

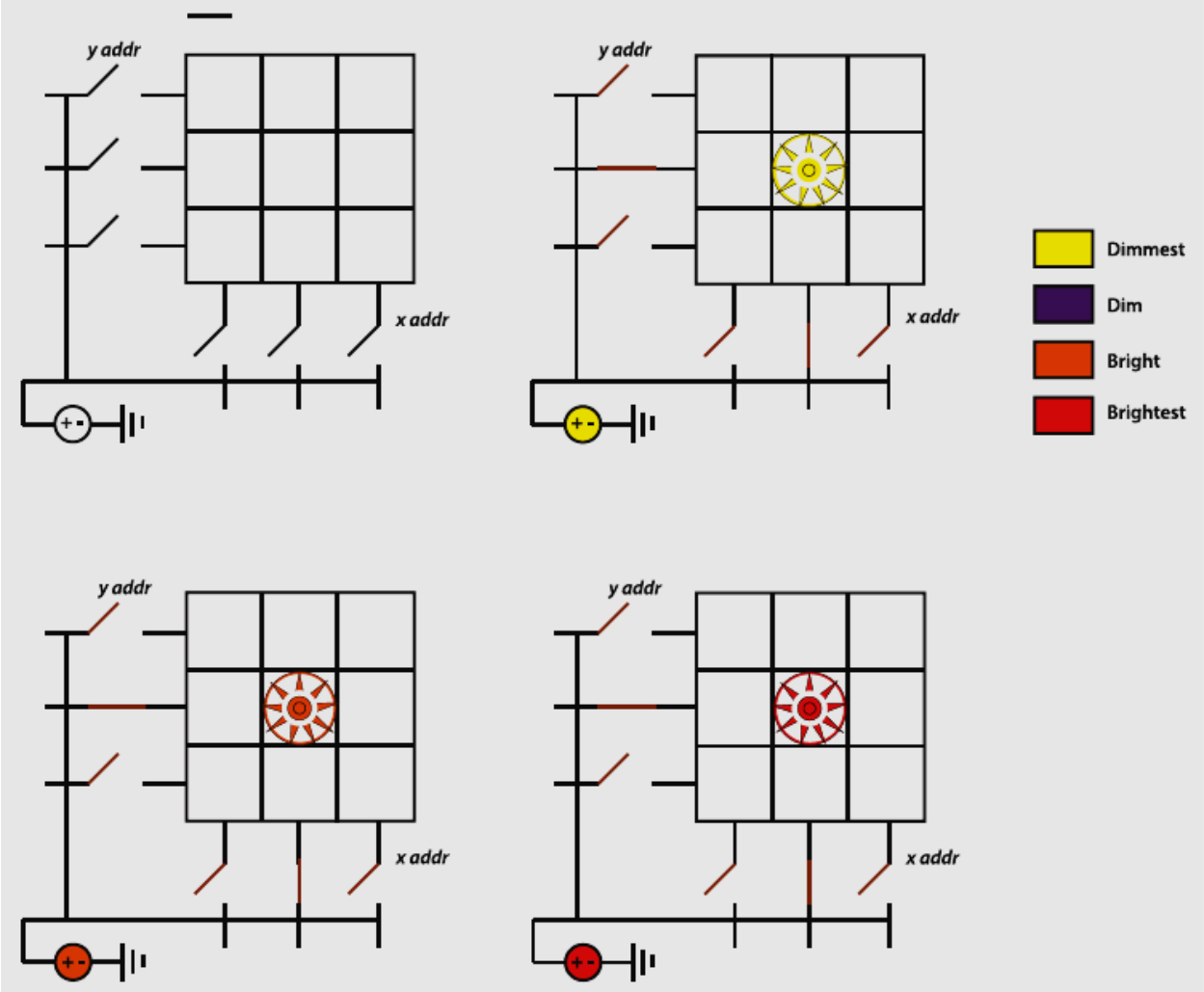

Figure 2.1: An example of a 3 x 3 pixel RIIC

Closing the appropriate switches for x and y locations applies a voltage to a specific LED which causes the pixel to light up.

Changing the brightness of the system falls to two components, the amplifier and the digital to analog converter (DAC). The DAC supplies an analog current signal, which takes a 16-bit digital input and turns it into a corresponding output current. This signal is then taken by the amplifier and converts the analog current into a voltage signal at a set range. This allows for the brightness of the pixels to be controlled by a digital signal

instead of an analog input. For example, sending all zeroes to the DAC will cause a pixel to deactivate, which can be seen in figure 2.2

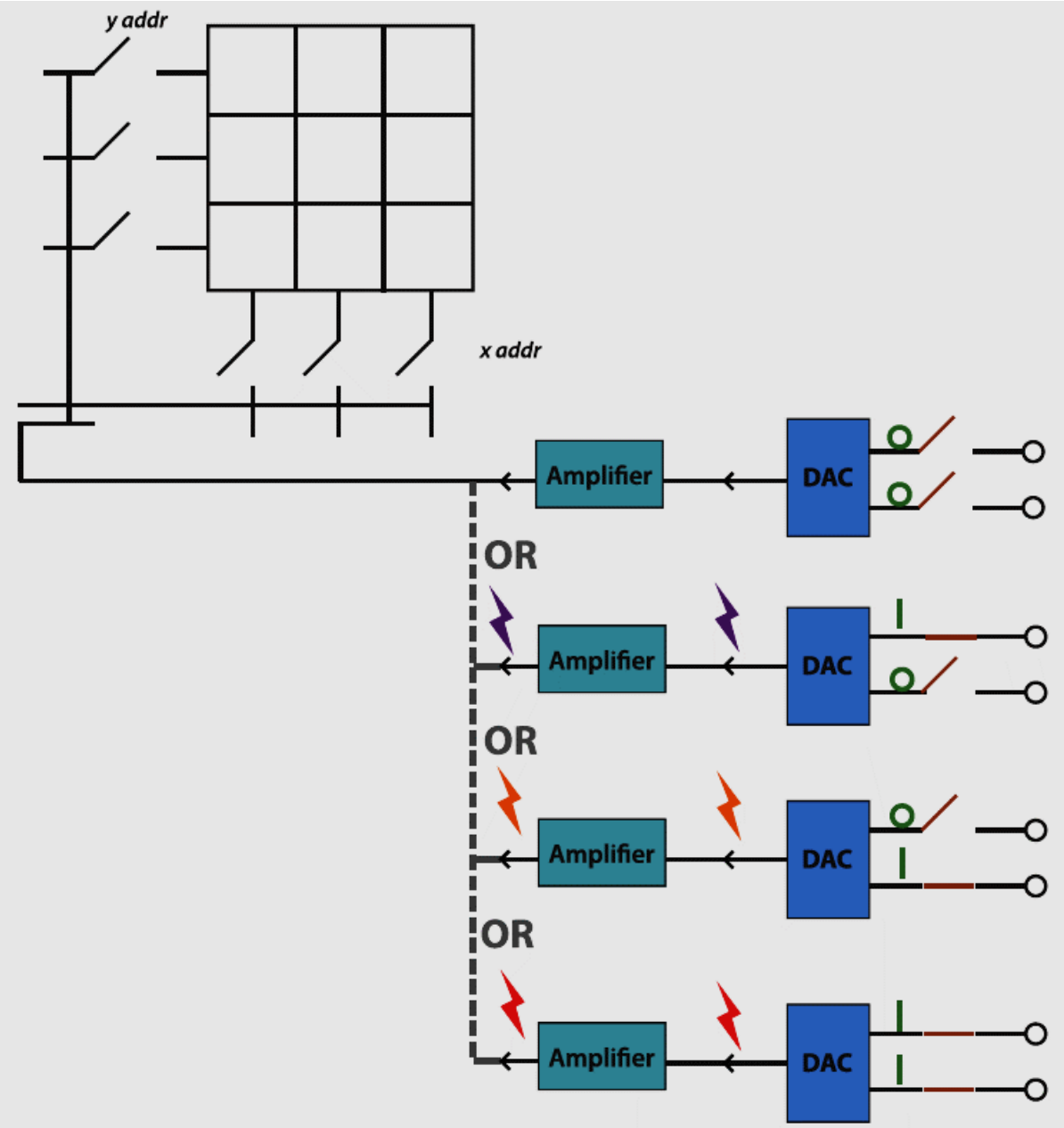

Figure 2.2: Digital input logic for the DAC, amplifier, and RIIC

The next stage is a Xilinx ML605 field programmable gate array (FPGA) board. This board is used to determine where the binary signal and the address of the pixel come

from. It controls the addressing and digital signals by using a hardware description language (HDL). In order to have all of the components of the system to communicate, an interface board was required. This interface board is connected to the DAC, amplifier, and RIIC through the outputs of the FPGA. The FGPA utilizes a component called Microblaze, which lets the user program it by using the C programming language, and some custom digital logic on the FPGA. It then becomes possible to tell each, individual pixel when to turn on and with what intensity. Figure 2.3 shows the connection between the RIIC, DAC, amplifier, and FPGA board.

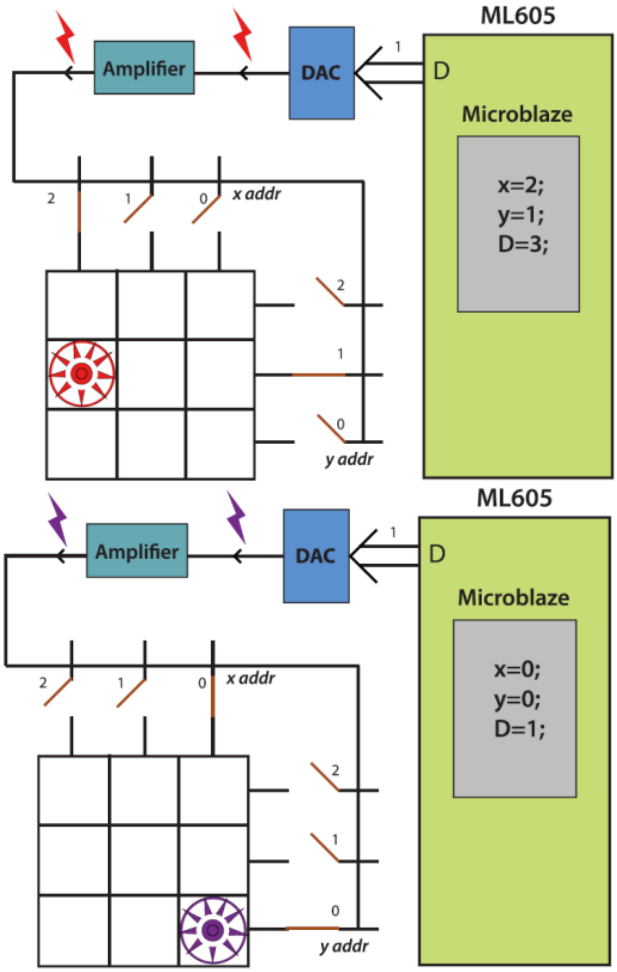

Figure 2.3: The ML605 FPGA driving the system

Additionally, instead of writing C code it is possible to send imagery to the FPGA through a DVI input. This allows a user to select a desired image to be projected and pass it through the FPGA board which will be displayed by the pixels. An example of the DVI setup can be seen in figure 2.4.

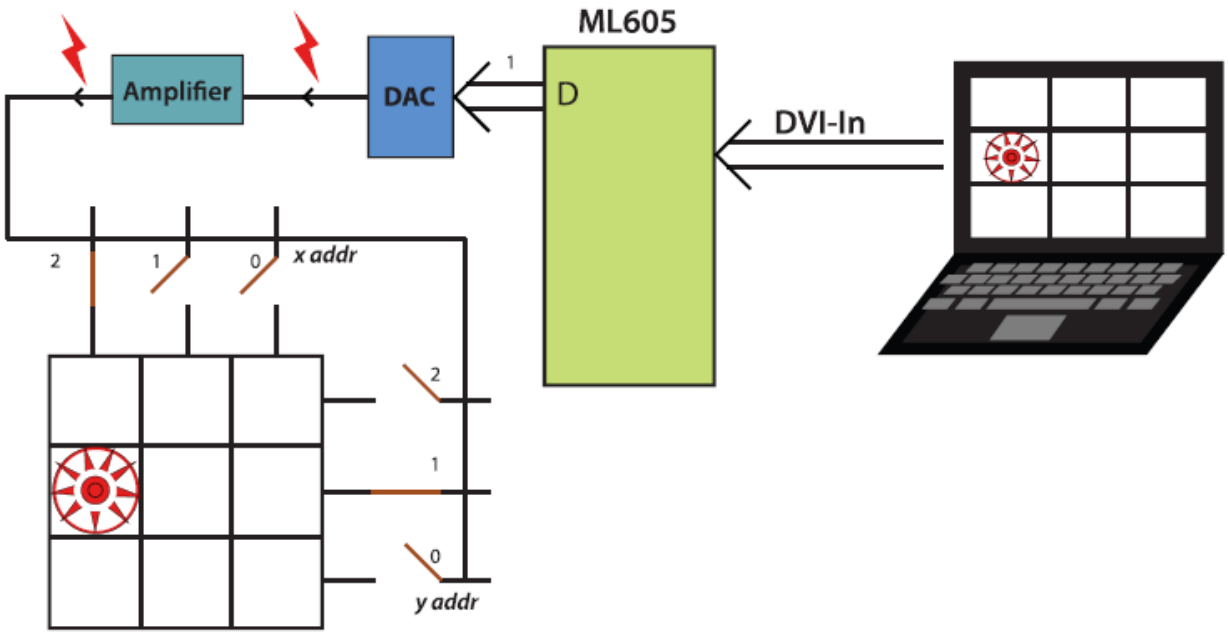

Figure 2.4: Displaying an image through the DVI input, to the FPGA, then to the SLEDs array

Chapter 3

SYSTEM COMPONENTS

3.1 Pixel

Every LED consists of 10V CMOS pass transistor pairs, which pass the analog input to the drive transistor and can be seen in figure 3.1.

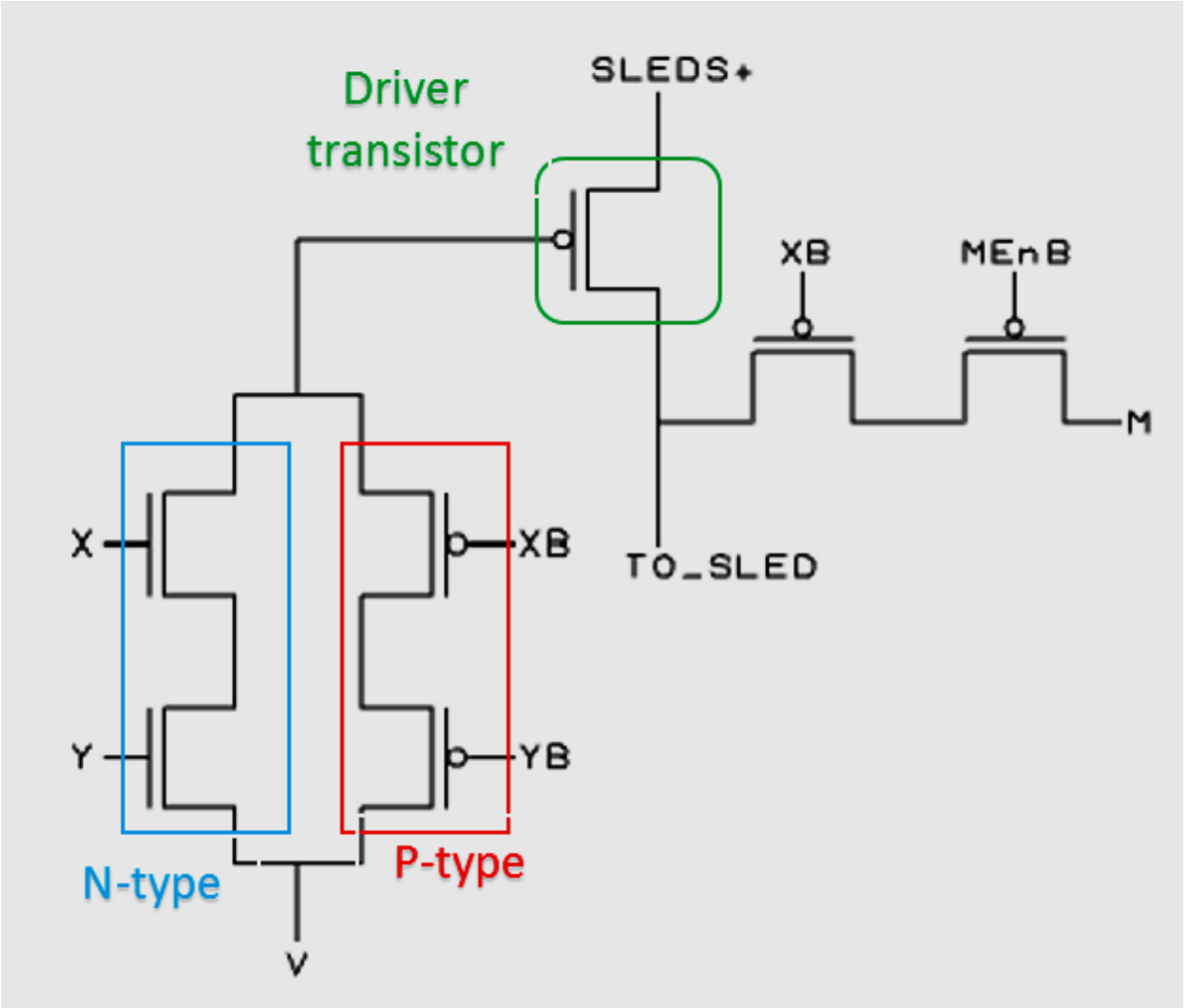

Figure 3.1: The schematic for a single pixel

These pass transistors are composed of both N type and P type metal oxide semiconductor field-effect transistors (MOSFETs) that are in parallel. These can be used to pass both high and low voltages with little to no issues. As an example, to turn on a

pixel at a high intensity both XB and YB need to be used. The two transistors, XB and MEnB were added to the pixels in order to be able to test the LEDs.

3.2 Read in Integrated Circuit (RIIC)

The read in integrated circuit (RIIC) is the LED driver. By using an external signal it is possible to control each LED through the RIIC. By using On Semiconductor's C5N process [5] it was possible to create a three metal, 0.5 µm CMOS process, and lateral high voltage transistors. Every LED driver circuit occupies an area of 48 x 48 μm^2, matches the SLEDs array, and connects to the LED anode and cathode terminals using 15µm high contact pads with indium bumps to minimize the thermal and electrical impedance between the SLEDs and the RIIC [6], which is shown in figure 3.2. The combination of the SLEDs and the RIIC via flip-chip bonding is called the hybrid.

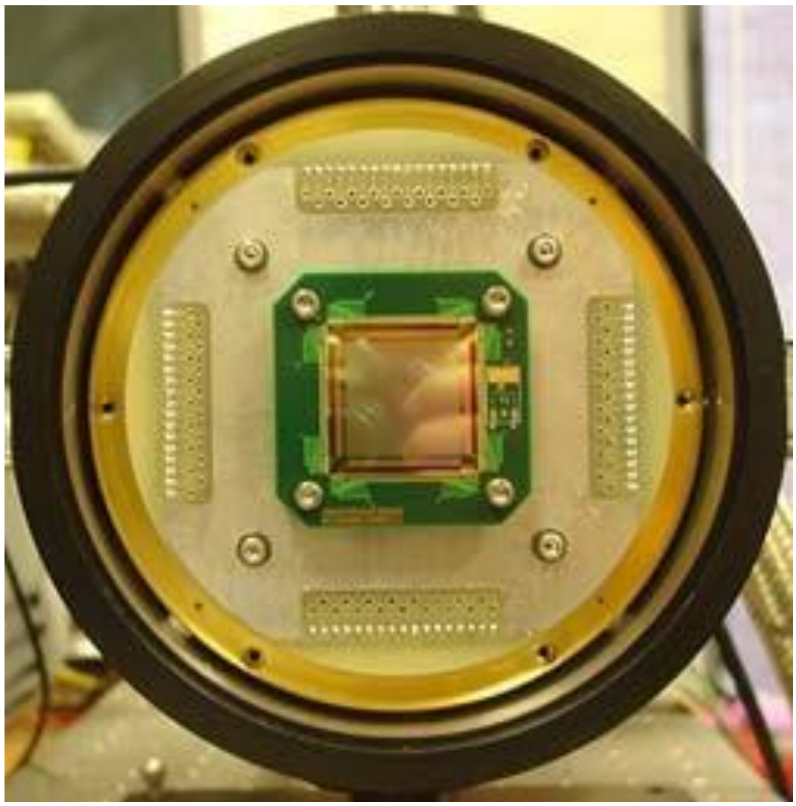

Figure 3.2: The RIIC mounted in a Dewar chamber

For the SLEDs to operate efficiently, they need to be kept at about 77 degrees Kelvin. To reach that temperature, the hybrid is packaged inside of a Dewar chamber, a device with a vacuum chamber attached to a reservoir for liquid nitrogen. The hybrid is placed in the vacuum chamber and connected to the liquid nitrogen by a metal block called a cold finger. The cold fingers' job is to move heat from the hybrid to the liquid nitrogen. However, this prevents immediate communication, electrically speaking, with the hybrid as the hybrid becomes sealed inside of the Dewar. To counteract this, a printed circuit board (PCB) was designed and fabricated to perform this job. The board contains 20 digital lines, 4 analog lines, and several power lines [7]. This board is called the Dewar board. The Dewar board connects to 50 ohm coaxial cables that run from the vacuum chamber along the liquid nitrogen reservoir to a set of headers on the back of the Dewar. The pin layout of the Dewar can be seen in figure 3.3. To address each pixel in the 512 x 512 RIIC, it would require 9-bit address lines. Each quadrant on the RIIC is electrically independent. There are 4 pre-charge bits that select the desired quadrant. Reducing the addressable array to 256x256 pixels. A 256x256 pixel array requires 8-bit x and y address lines. There are 4 analog inputs that enable the writing of 4 pixels at once – one in each quadrant.

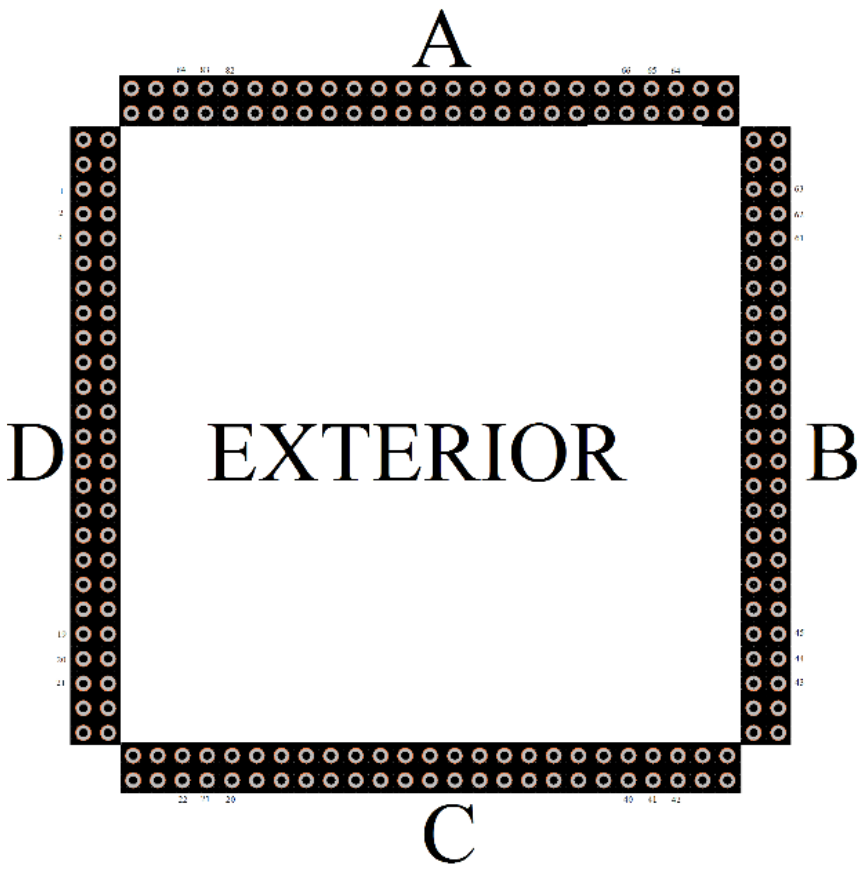

Figure 3.3: The pin layout of the Dewar

3.3 ML605 FPGA

The ML605 field programmable gate array (FPGA) is one of the most, if not the most, important component in the projector system. It allows for the connection of the hardware and software interfaces. Additionally, it allows for the drive signals to be programmed depending on the desired outputs. To do this, Xilinx, the manufacturer, provides software that allows a user to program the FPGA. This software is comprised of two main components, the software development kit (SDK) and the embedded development kit (EDK). The SDK is used to create VHDL peripherals while the EDK uses the VHDL language to develop the system firmware. An example of the FPGA is shown in figure 3.4.

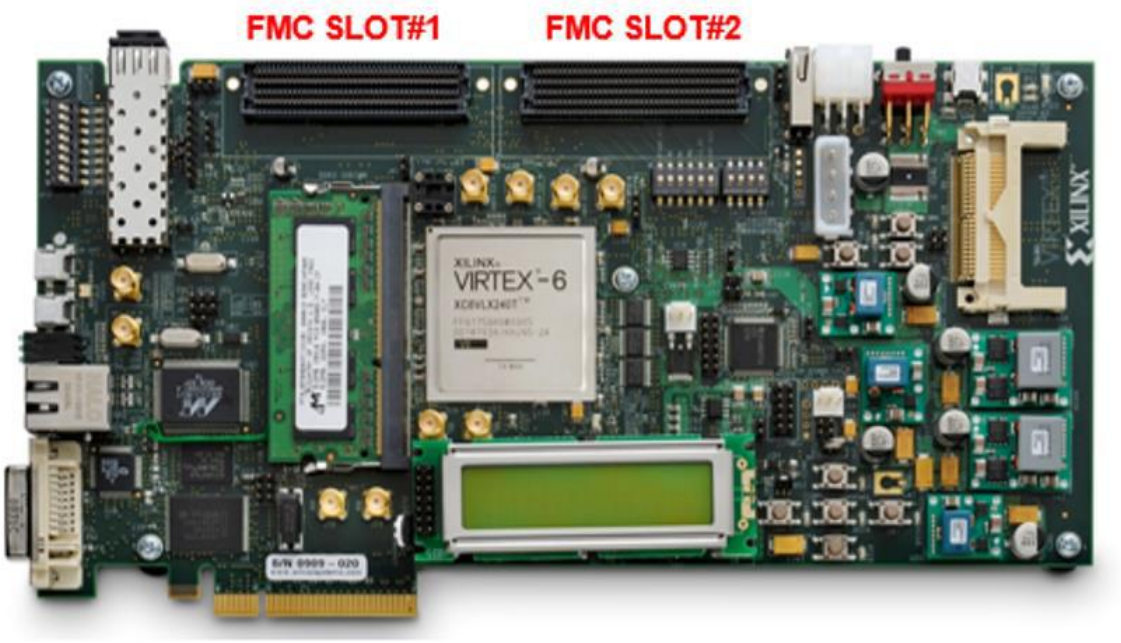

Figure 3.4: The ML605 FPGA

The two FMC slots both run the system through the DVI cable and are used for debugging purposes.

3.4 Analog Amplifier

The LEDs require a voltage as an input which requires an amplifier. This voltage needs to be high speed and low noise, so an analog amplifier was custom designed and fabricated. The amplifier uses a TH6012 op-amp by Texas Instruments which is used to amplify each output current line from the evaluation board to the correct voltage level. The SMA connectors on the board are used to transmit the output of each channel to the interface board [8]. This is to account for the highly capacitive load of the SLEDs hybrid as the design has a tunable RC snubber for output edge damping [9]. The amplifier board is shown in figure 3.5.

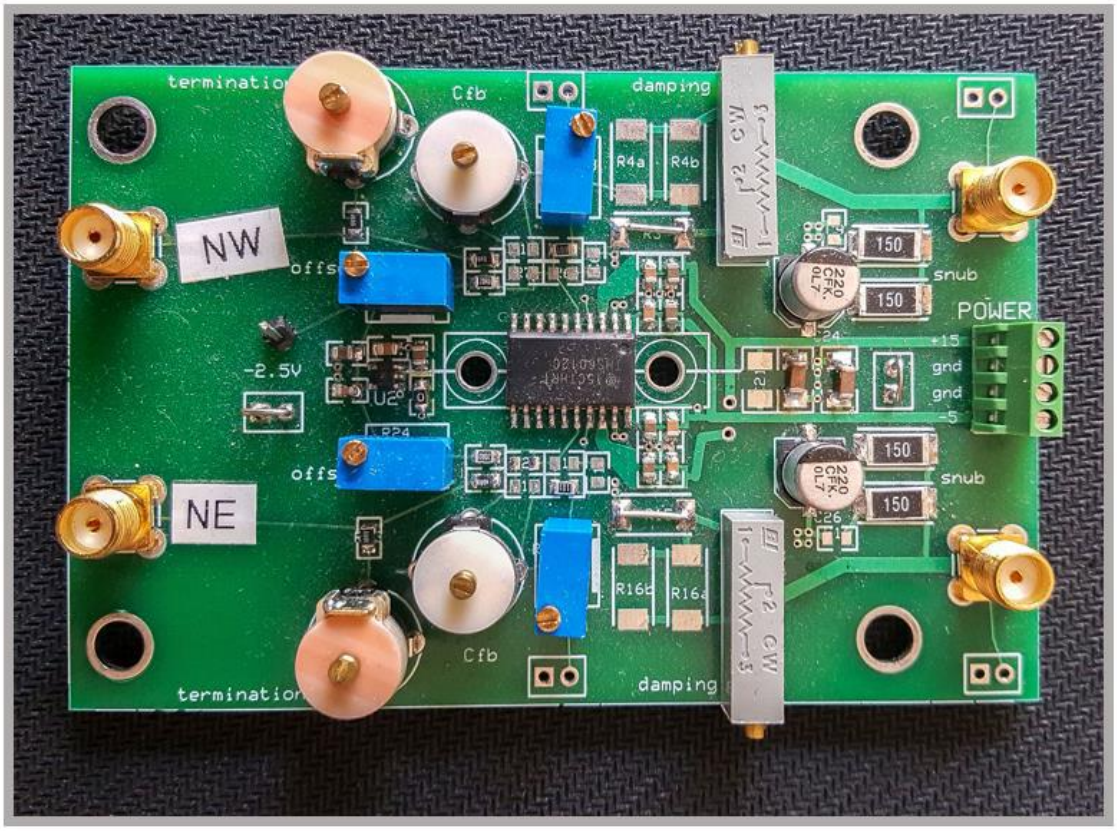

Figure 3.5: The amplifier board

3.5 Interface Board

The interface board, shown in figure 3.6, is what allows each component to communicate with each other. It requires 10V to 12V of power, which it uses to power on the RIIC, DAC amplifier board, and DAC evaluation board. It also connects to the ML605 FPGA, which is what allows for the shifting of the digital lines from 2.5V to 5V. Additionally, connecting to the FPGA makes it possible to use the FPGA to monitor the amount of current that is drawn and can act as a virtual circuit breaker. All of the signals are routed to the Dewar through the use of ribbon connectors that attach to the connection pins that go into the Dewar.

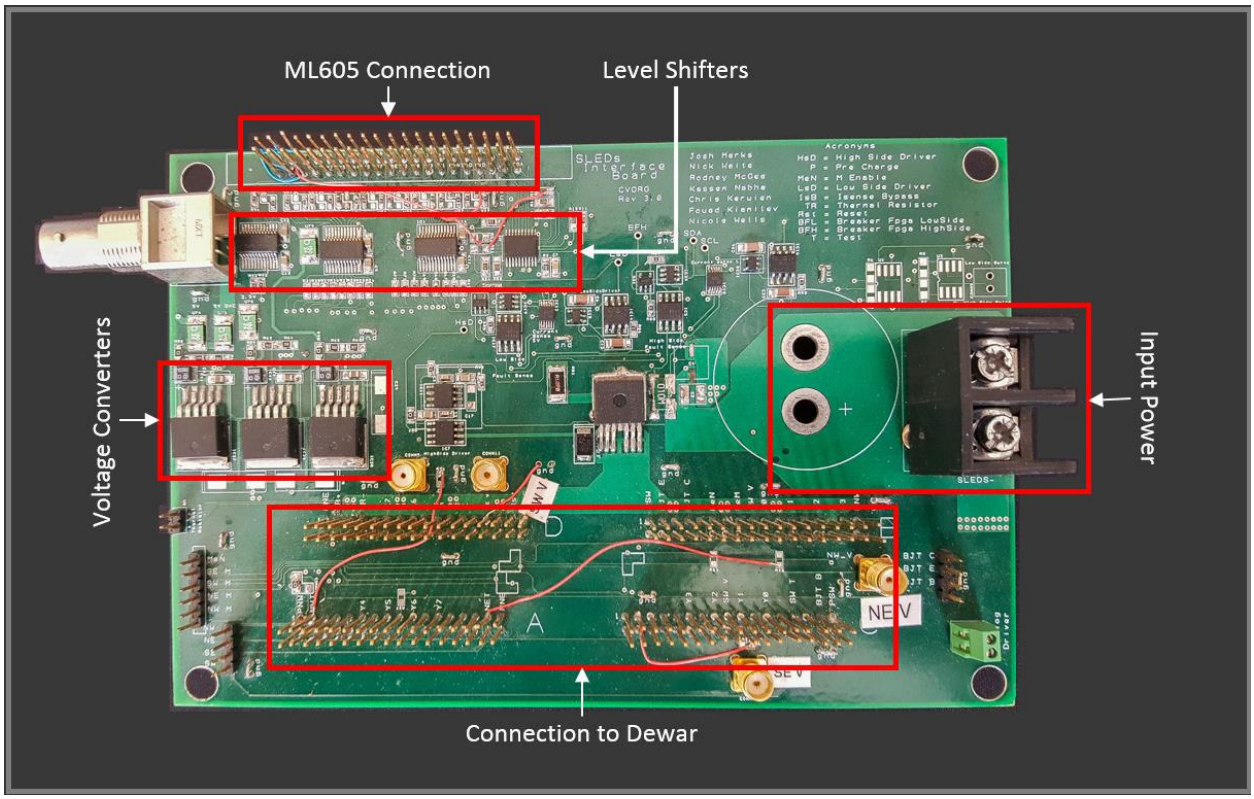

Figure 3.6: The interface board

3.6 AD9747 Evaluation Board

The evaluation board makes use of an AD9747 dual DAC chip, which is manufactured by Analog Devices and can be seen in figure 3.7. The evaluation board was selected as it has a dynamic and high range while giving a useful output current. The output current is used to control the LEDs in a digital manner. More information can be read about in Kerwien's thesis [10].

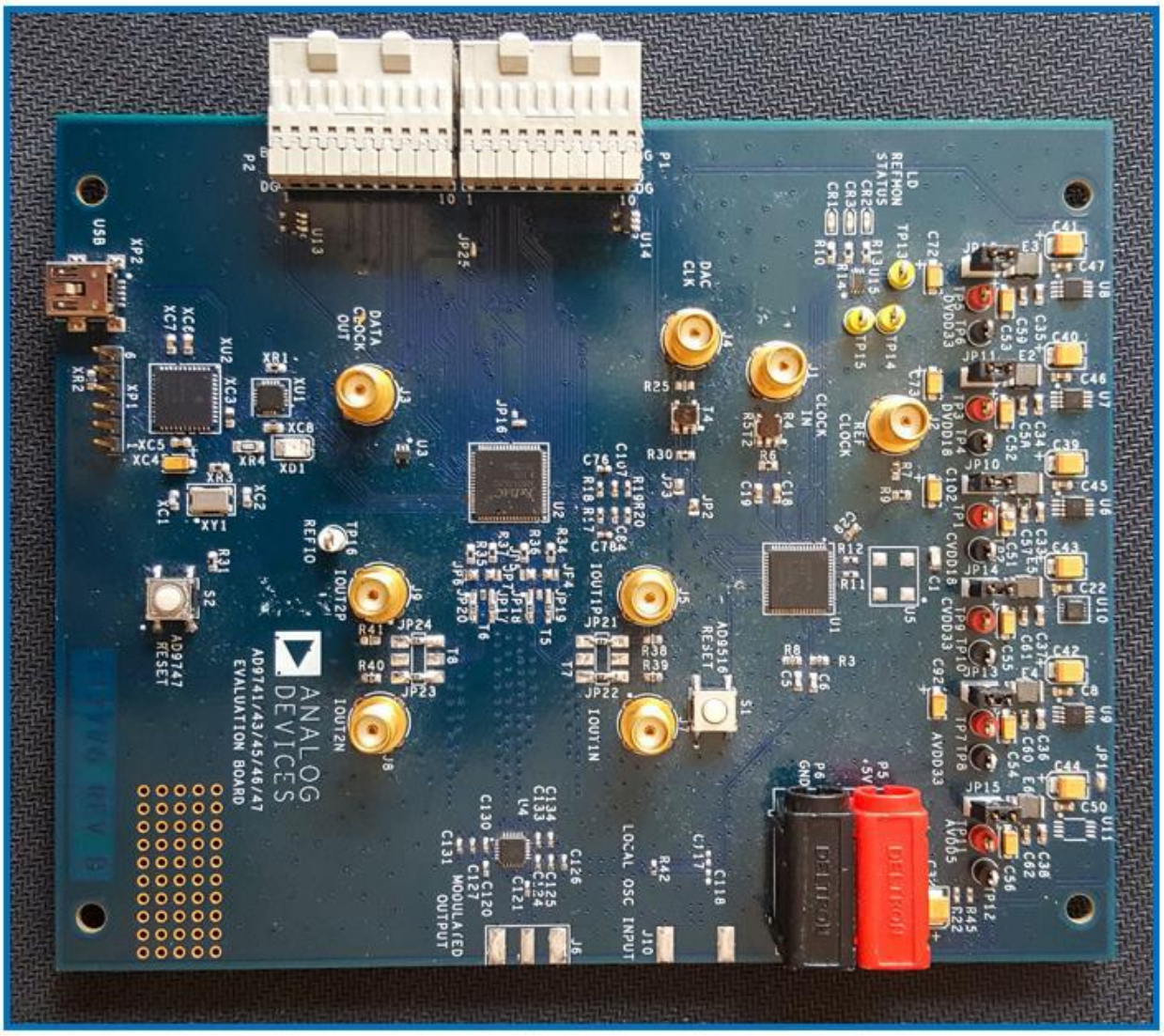

Figure 3.7: The evaluation board

3.7 IR Camera

In an ordinary projector, visible light would be emitted at the system output. However, since these are IRLEDs, instead infrared light is the output. This type of light is not visible to the human eye and as such requires an infrared camera to see.

The system uses a FLIR SC8200 camera. The model operates in the 3.0 – 5.0 µm range with a resolution of 1024 x 1024 and a detector pitch of 18µm. The camera is

operated through Ethernet and camera link but it can also be controlled through USB and RS-232. A picture of the camera looking at the Dewar can be seen in figure 3.8 [11].

Figure 3.8: The FLIR camera looking at the Dewar

The provided software is limited as it can only take single frame images. In order to work around this limitation, the system incorporates a capture card. This enables the rapid acquisition of still images to make a video at a rate that suits the project needs. The card used is a Vision Link F4, which is a 4-lane PCIe frame grabber with two camera link connectors. It has a 256MB internal memory that is used to store the images for fast camera capturing [12].

3.8 The Complete System

The complete system can be seen in figure 3.9, which is how the system works together as more than a collection of parts.

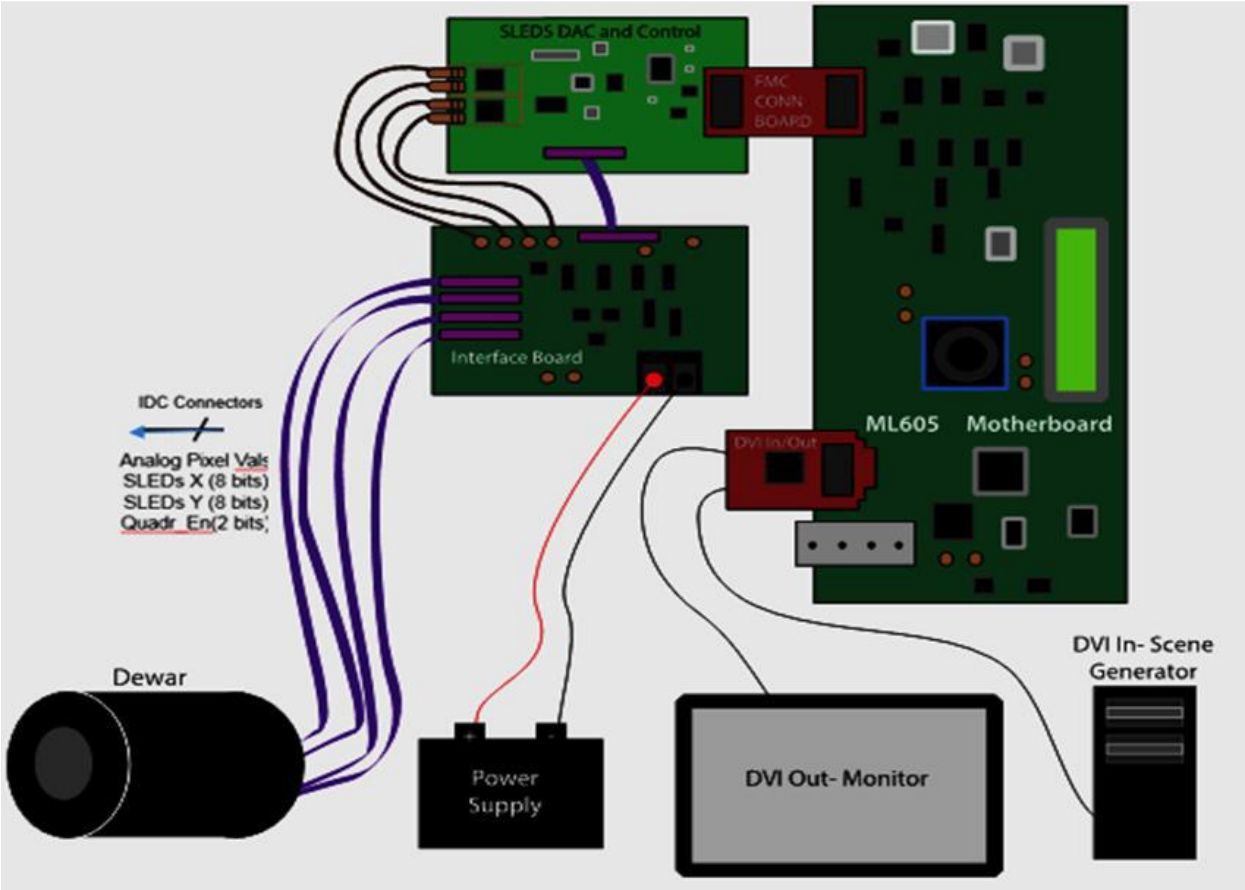

Figure 3.9: Graphical representation of the complete system

The system has a power supply which provides power to the interface board which is used to light up the entire pixel array. The pixel array is housed inside of the Dewar which helps cool the chip down. The chip is cooled because the LEDs are extremely inefficient and have a 99.7% power loss to heat. This is a limitation due to the technology of LEDs themselves.

Chapter 4

PACKAGING AND THERMAL PROBLEMS

4.1 Current Packaging

The packaging that is currently in use is a JK CTS-1260 Dewar chamber by J.K. Henriksen, as seen in figure 4.1, which is the most practical type that is available on the market.

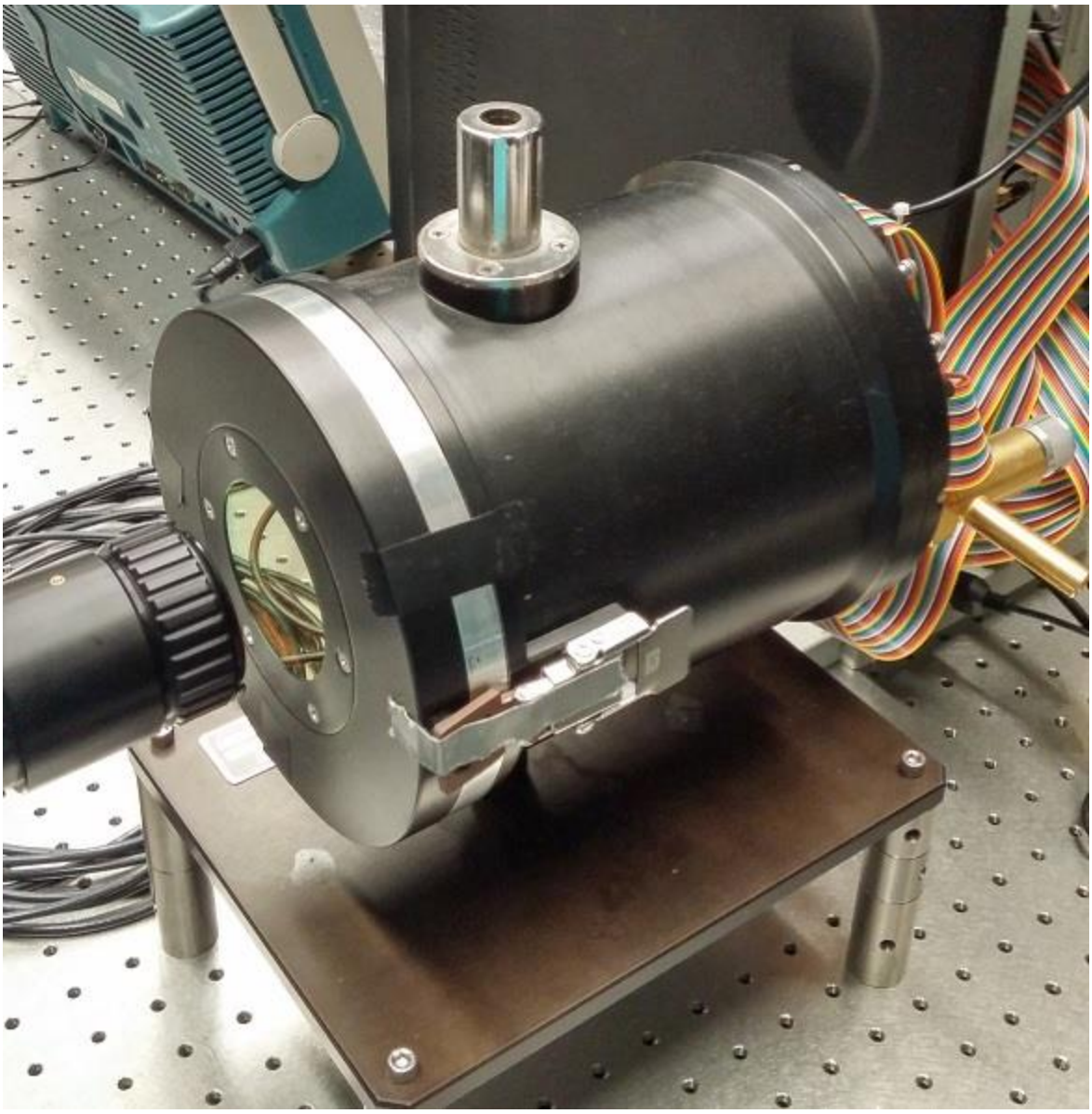

Figure 4.1: The current pour filled Dewar in use

The packaging is meant to achieve two things; to keep the chip cold and under vacuum. Keeping the chip at cryogenic temperatures helps to increase the efficiency of the LEDs. The chip, an array of LEDs, operates at 0.03% efficiency rating. This means that 99.97% of the energy used by the LEDs is displaced as waste heat, between 20 to 30 watts. As the heat of the system rises, the performance correspondingly drops, as can be seen in figure 4.2.

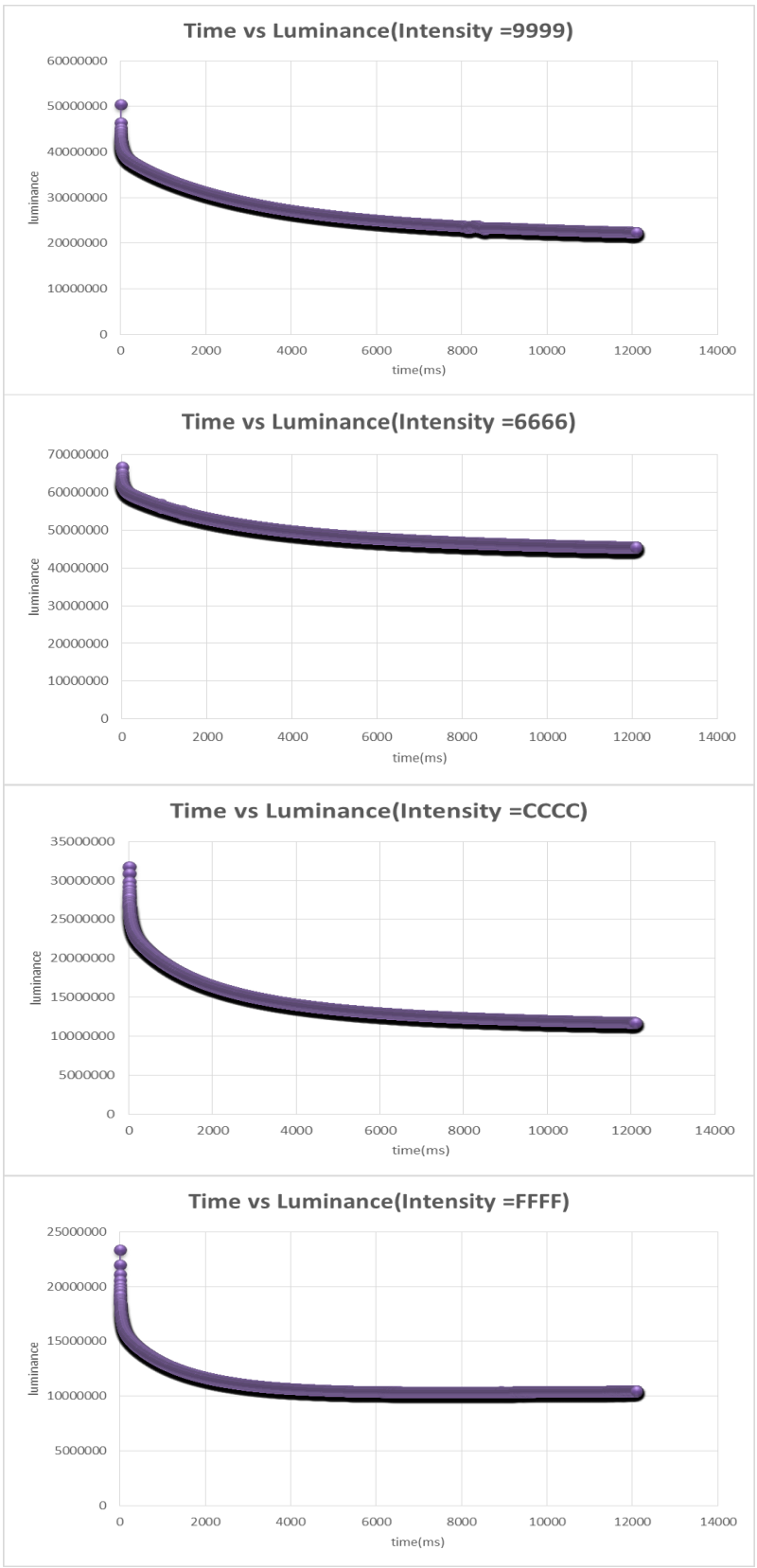

Figure 4.2: These graphs show the time vs normalized luminance at different intensities counts in hexadecimal

The test to determine figure 4.2 was done by lighting about 75 pixels and keeping them on for 120 seconds with a 5-minute rest period between tests. The rest period ensured that heat from the previous test was properly dissipated before beginning again. These figures show that as time goes on the pixels lose luminance faster and faster. This is believed to happen because the current cryostat does not remove heat fast enough from the SLEDS array [13].

4.2 Current System Drawbacks

Currently, the two major types of Dewars that are available on the market are a pour-filled tank or an impingement styled jet. Both styles use liquid nitrogen as their cryogen, which has been reliable in many other low temperature applications. The main difference in the two types of Dewars are the ways in which liquid nitrogen is delivered to the system. The pour filled type uses a chamber that is filled with liquid nitrogen and uses the low heat of vaporization to boil off nitrogen and remove heat passively [14]. The jet impingement type of Dewar uses a steady stream of liquid nitrogen directed at a cold finger to remove heat from a chip. This method requires a way to pressurize the nitrogen to dispense it in a jet. Both types of systems will be covered more in depth in the next sections.

4.2.1 Pour Filled Dewar Chamber

The pour-filled chamber takes advantage of the low heat of vaporization [14]. This causes the liquid nitrogen to boil off very quickly, taking energy with it. The downfall of this method is that, due to the nature of the design, there is no efficient way for the nitrogen vapor to leave the system. There is a silver exhaust pipe at the top of the chamber, however this does not allow for a fast-enough evacuation of the vapor. In turn,

this causes a pressurized vapor barrier inside of the tank. This vapor barrier prevents the liquid nitrogen from interacting with the cold finger of the device, limiting the amount of heat that can be removed. In order to remove heat from the system, it must undergo conduction through the cold finger to the vapor and then conduction from the vapor to the liquid nitrogen. The conduction from the cold finger to the nitrogen vapor is incredibly slow when compared to the more direct process of conduction from the cold finger to the liquid nitrogen. This is because the amount of energy that nitrogen vapor can absorb is much less than that of liquid nitrogen, so this in effect becomes a bottleneck.

4.2.2 Jet Impingement Cooler

The jet impingement type of Dewar uses a pressurized stream of liquid nitrogen shot at the cold finger to dispel the vapor barrier that plagues the pour filled Dewar chamber, an example of which can be seen in figure 4.3.

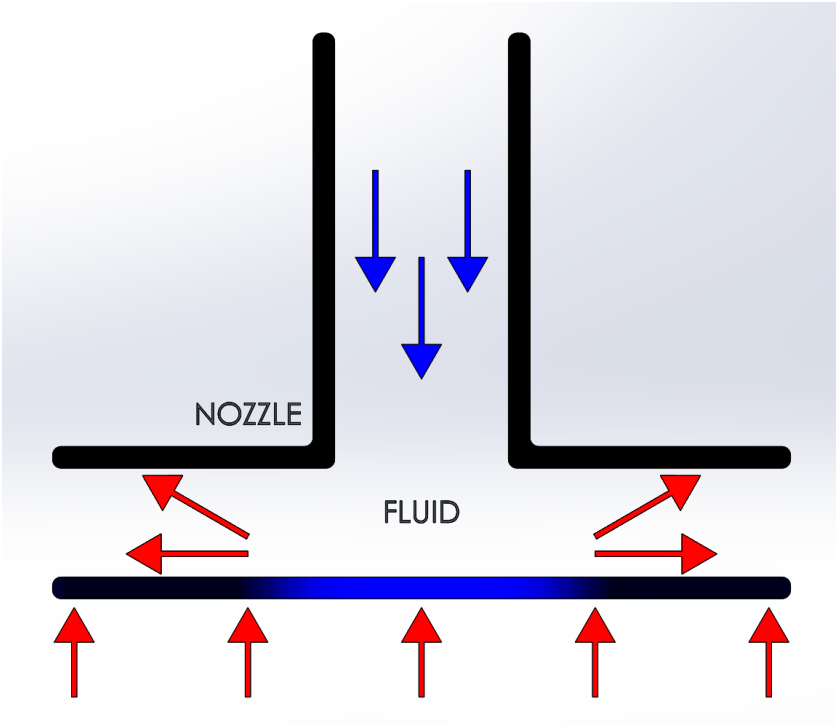

Figure 4.3: The basic principle of jet impingement cooling

At first glance, this appears that it should solve the problem and be a sufficient solution. The diameter of the jet is far too small to satisfy the hybrid sizes that are currently in use. For smaller sized hybrids, this would not be a problem, however for the IRSPs, larger hybrids were necessary in order to deliver on the higher framerate and resolution. For example, HDILEDs uses a 2" x 2" chip size. The jet does not cover a large enough surface to be effective as it can only reach the center of the chip but leaves the edges uncooled. This thermal imbalance can cause a large amount of damage to the chip if left unchecked as it could cause physical warping of the chip and even cracking if left on for too long.

4.2.3 Common Problems

In addition to the heat removal problems that were previously discussed, both Dewar chamber types suffer from common problems in the same manner. For future generations of the IRSPs, scalability is an incredibly important capability. The system must be able to grow as large as necessary to attain its goals. The Dewar chambers themselves limit this scalable growth in several ways. They were never truly designed to accommodate chips as large as the SLEDs chips so they have limited input/output (I/O) pins, introduce large transmission lines that are inherent to the system, and limit the chip size due to how the chip is held in the chamber itself.

The Dewar has 100 I/O pins inherently built in to the system. Normally, for the chip size the chamber was designed to accommodate, this would be more than enough. However, the SLEDs chips, in their current states, can require upwards of 400 pins [15], depending on the hybrid that is being tested. The design dictates that the hybrid be attached to a PCB that can be screwed into place according to a bolt pattern in the Dewar

chamber. From that PCB, a series of spring contacts are attached to internal cables and run to the back of the device. This allows for the holding of a vacuum, as cables are not breaking a seal by exiting via the sides of the chamber, as can be seen in figure 4.4.

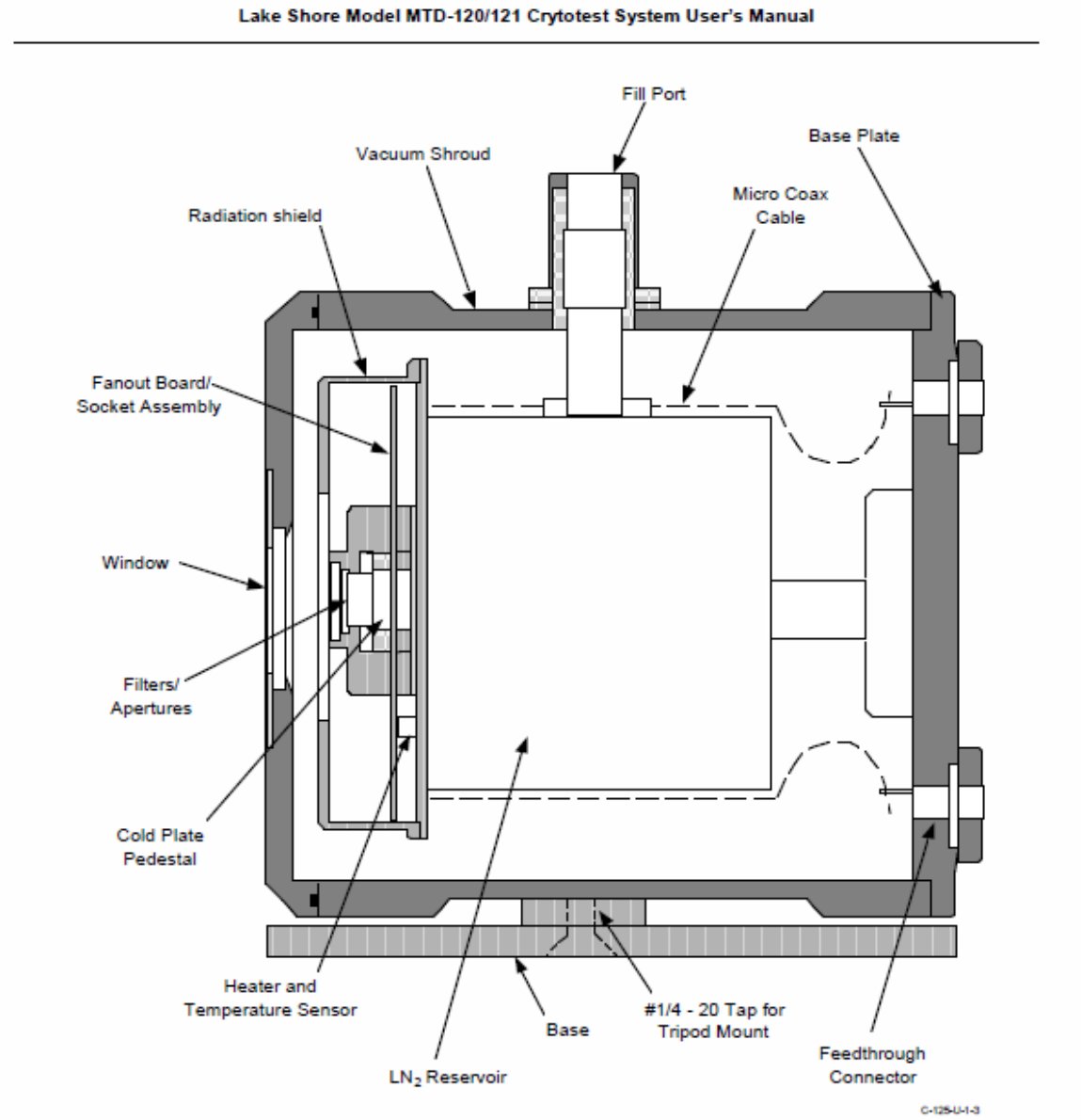

Figure 4.4: A cutaway view of the J.K. Henriksen Dewar chamber showing how the chip is mounted inside and has feedthrough connectors coming out of the back of the device, labeled micro coax cable.

The addition of these internal cables along with the PCB traces, while necessary, added a large impedance imbalance to the system. There is no practical way to reconcile these mismatches as they are from the physics of the setup. The large mismatch disrupts the signal as it echoes between the source and destination of the chip. This echo prevents the data acquired from truly being a 16 bit signal at the output.

The currently available Dewar chambers are not sufficient for the current projects due to a lack of scalability, among other problems. The design of the Henriksen Dewar chambers will, in many cases, work for smaller scale projects. However, due to the nature of the SLEDs chips, they are limited by the capabilities of the current Dewar chamber. The size restriction of the Dewar chamber prevents the future designs of the hybrids from getting larger as there simply isn't enough room.

Chapter 5

RESULTS

5.1 Custom Cryostat

In order to solve the previously discussed problems, it became necessary to determine a completely new way of packaging the SLEDS chips. It was determined that simply building, or ordering, a larger version of the same type of Dewar chamber would not solve the scaling problems indefinitely. At its current resolution of 512x512, the HDILEDs chip is a 2" x 2" square and the final resolution of this chip will be even larger. It would not make economic sense to custom order larger and larger Dewar chambers that have so many limitations. To determine a design that would allow for unlimited scalability, a few questions had to be answered. How to hold a sizable vacuum on a variable size hybrid? How to eliminate the transmission lines? How to increase the rate of heat removal? After doing some initial research, it was found that holding a vacuum, about 10^{-3} Torr, while using a PCB as a sealing wall was feasible. This led to the construction of a vacuum test chamber, the plans for which can be seen in figure 5.1.

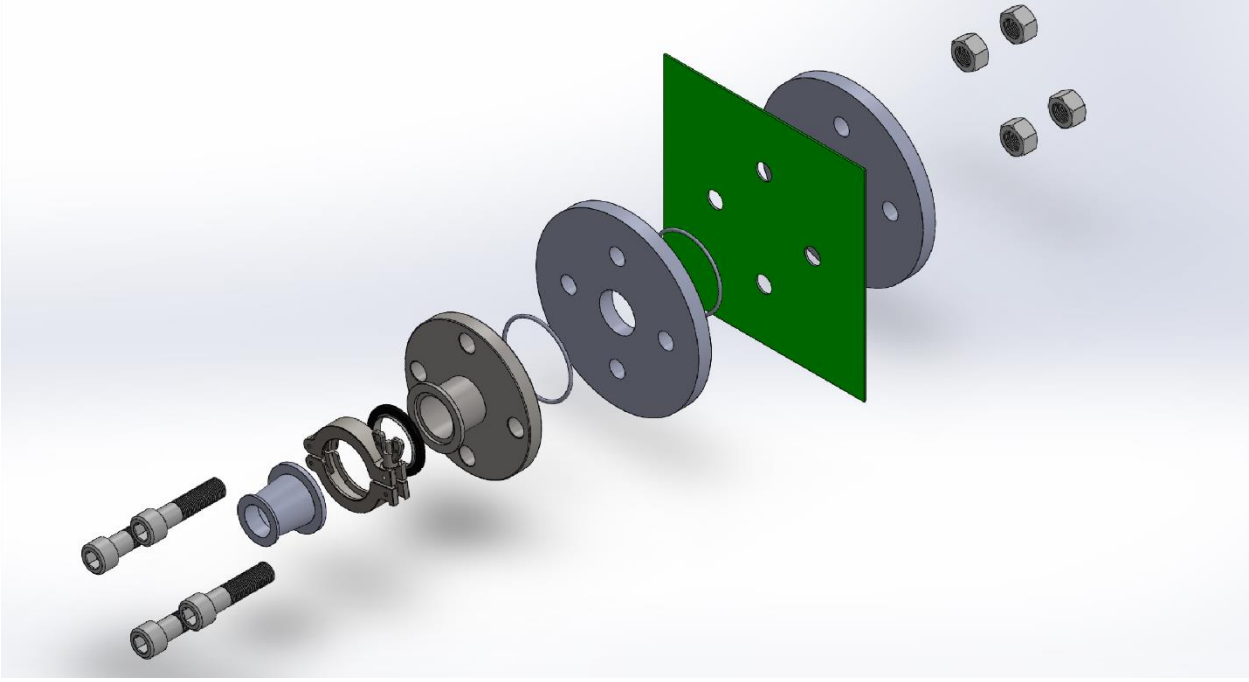

Figure 5.1: The 3D exploded model for a custom-built rig to determine if holding a vacuum while using a PCB as a chamber wall is feasible.

The design that was chosen to solve these problems was a two-part approach. The two parts were a vacuum section and a cooling section, each would require their own solutions as each proposed their own problems. An outside company would handle the cooling section of the chamber, *ARS Cryo*, as their specialty is designing custom, research lab based, cryostats. Details of their involvement are in the following sections.

The vacuum chamber section had to allow for virtually unlimited scalability while keeping impedance mismatches to a minimum. This meant that the chamber had to be able to accommodate a large PCB and chip without the use of lengthy feedthrough cables. These problems were solved in one design choice. The idea was to use the PCB itself as a vacuum wall and simply have electrical connections to the part of the PCB that was already outside of the vacuum chamber. This meant that any size board could be slotted into place and that there would be no transmission lines as there would be no

cables between the board and the interface computer. This was achieved by sandwiching the PCB between two plates with O-rings in between.

After the initial design stage, the device needed to be tested. The device was subsequently manufactured and tested in two configurations. The first configuration was holding a vacuum on one side of a PCB that had been baked out to about 125°C for 30 minutes [16], as can be seen in figure 5.2.

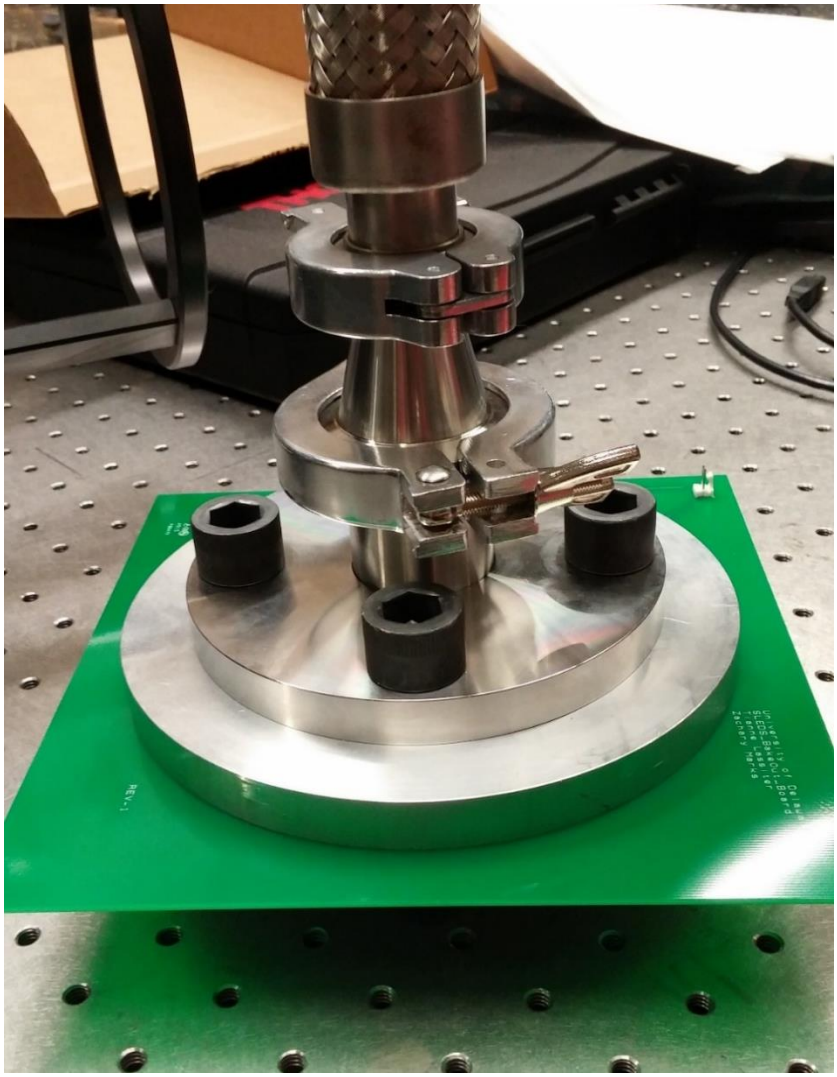

Figure 5.2: The testing rig to determine if holding vacuum against a PCB was possible.

This was done as the fiberglass that largely makes up PCBs is porous and contains several volatiles in the material itself. During a pump-down with a vacuum pump, these volatiles would become free due to the lower pressure and cause false readings on a pressure gauge.

The second configuration of the testing rig was the addition of a glass window at the bottom of the device as well as a hole put into the center of the PCB. The window was to determine if it was possible to have both sides of the PCB hold a vacuum as this would be closer to the finalized product, which uses an optical window. The hole in the PCB was to allow gas to move from the window side to the pump port side of the chamber, effectively doubling the chamber volume. This brought the testing rig closer to the finalized product as the PCBs that hold the chips will have several holes around it to allow for the movement of gas. The plans for this can be seen in figure 5.3 and the modification can be seen in figure 5.4, respectively.

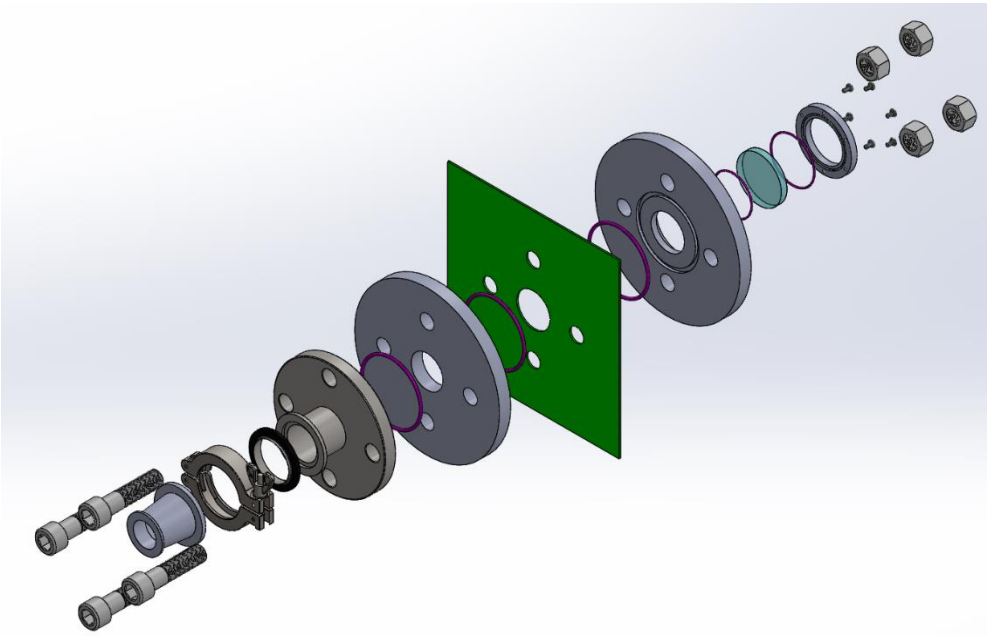

Figure 5.3: The exploded view of a 3D CAD model for the addition of a window.

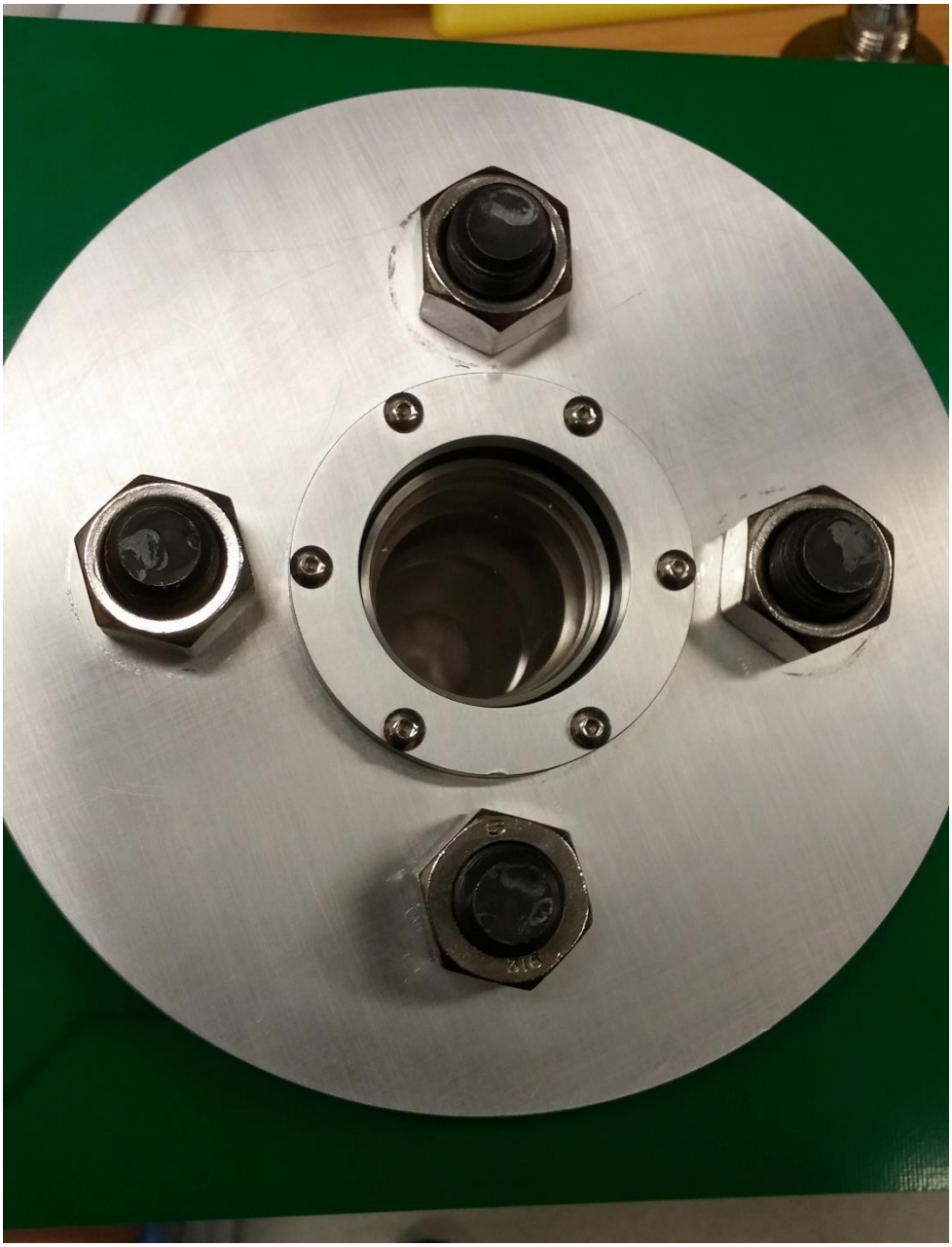

Figure 5.4: The addition of the window to the bottom of the device.

Two types of tests were conducted to determine if the device leaked or not. The first type of test was a basic monitoring. The device would be brought to vacuum at about 10^{-3} Torr over the course of a few hours. Once the device was at the appropriate vacuum level, the pump was deactivated and a pressure gauge was used to monitor the internal pressure of the chamber. The gauge readout was monitored over the course of an hour to

have enough time to measure a significant enough pressure change, an example of which can be seen in figure 5.5.

Figure 5.5: The pressure gauge readout used to measure pressure inside of the testing rig.

The second testing method was to use a helium leak testing device, an example of which can be seen in figure 5.6.

Figure 5.6: An example of a helium leak testing unit.

The leak tester was used to determine if helium, a highly penetrative gas, could pass through any of the testing rigs' leak points. This was done by pulling vacuum inside of the device and using a wand that emitted helium gas at the fault points of the rig. If the helium entered the chamber at all, the attached sensor would find it and record the pressure changes. These fault points included all of the separate metal connection points as well as the window in the second test setup. It was found that, both with the window and without, the leak rate stayed well inside an acceptable amount. The leak rates were measured at $2 \cdot 10^{-9}$ mbars•L/s ± $1 \cdot 10^{-9}$ mbars•L/s. This indicated that in both configurations, the PCB successfully held a vacuum.

5.1.1 Finalized Design

The final design of the vacuum system took full advantage of the sandwiched PCB as well as including a few other design choices. A 3D CAD model can be seen in figure 5.7.

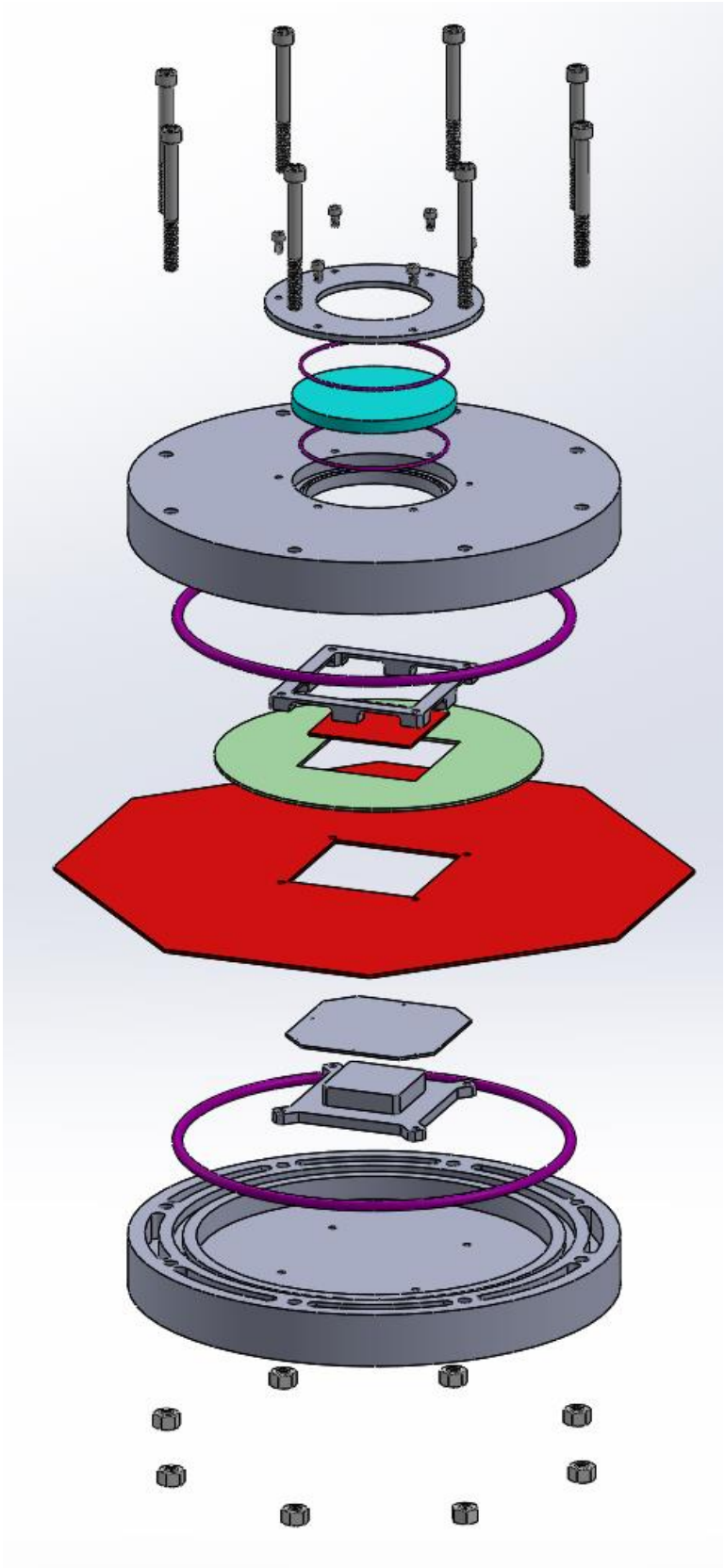

Figure 5.7: An exploded view of the finalized vacuum system concept

The discovery that a PCB could hold a sizable vacuum for a good period of time led to the eventual partnership with an outside company, *ARS Cryo*. They are a company that specializes in the creation of custom cryostats specifically for lab based research. They were chosen as they could provide a cryostat that would take advantage of using a PCB as a vacuum wall at a reasonable cost. The final concept will take advantage of compressing a PCB to attain a vacuum as well as a proprietary cooling device designed and manufactured by *ARS*. The device will use liquid nitrogen in a flowing system to remove heat from the chip. The largest difference is that this unit will have a much larger heat removal capability, about 200W of heat compared to the previous 20W of heat removal. This is achieved through a proprietary, single stage, heat removal system that was developed by *ARS Cryo*, which can be seen in figure 5.8.

Figure 5.8: The single stage heat removal system designed by *ARS Cryo*.

The device will be attached to a liquid nitrogen pump system which will circulate liquid nitrogen within the system in a closed loop. This will be achieved by the use of a compressor that will be attached with helium hoses, allowing for the cryostat to be mounted independently on a table, which can be seen in figure 5.9.

Figure 5.9: The compressor that will be used to flow liquid nitrogen in the cryostat.

This system can be fine-tuned to maintain a certain level of heat inside of the vacuum chamber, which will be mounted at the end of the copper section. The end of the copper section will be what interacts with the chip through the use of a cold head. This cold head will draw heat from the chip and disperse it through the rest of the cryostat.

The vacuum chamber of the custom cryostat will use the same principle, sandwiching a PCB between two O-rings, albeit in a slightly different form. The form change happened due to tolerances and machining capabilities from *ARS Cryo* and can be seen in figure 5.10.

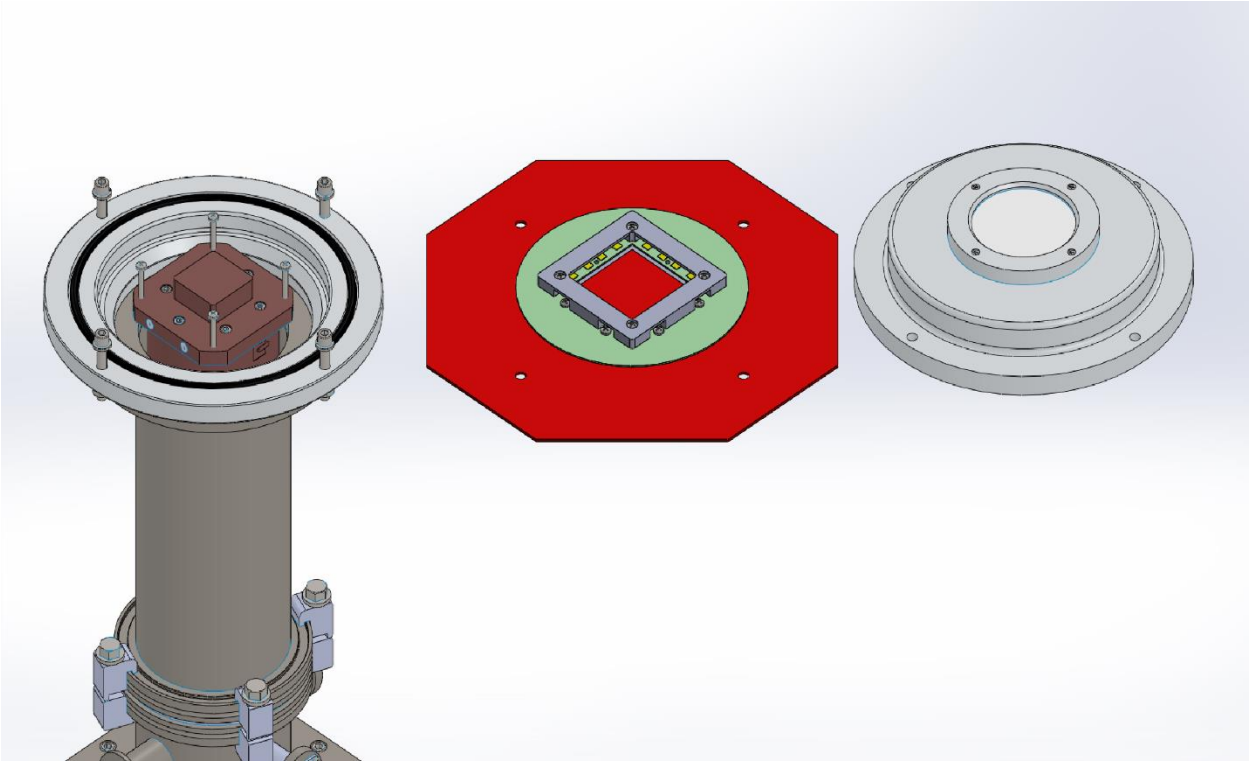

Figure 5.10: The internals of the cryostat that was accepted by *ARS Cryo* using the sandwiched PCB design.

5.2 Solutions to Current Problems

The custom cryostat will address each of the problems faced by the Henriksen Dewar chambers in a way that will allow for the next generations of IRSPs to be tested with minimal to no restrictions. The custom model, when compared to the current models, excel in the main requirements of heat removal, data transmission, and

scalability. These improvements are met through several requirements that all play in to one another.

The custom system can remove about 200W of heat, which is a tenfold increase from the previously used cryostats. This is achieved by the work of *ARS Cryo* and their cooling systems. The main drawback from the Henriksen Dewars are that they are not designed for a chip as large as HDILEDs and as such do not have large enough cold fingers. In the custom model, the cold finger will start by accommodating a 2" x 2" chip with the ability to be easily removed and replaced with a larger cold finger as necessary. This allows for any size of cold finger to be inserted, provided it uses a simple mounting bolt pattern. Additionally, the custom cryostat allows for different sized optical windows to be used as it becomes necessary. This is achieved by using a different lid that can hold a different optical window, meaning it is possible to have specific windows for different chips.

The custom cryostat eliminates unnecessary transmission lines between the chip and the outside world. By having the PCB extend beyond the vacuum chamber, this allows for any number of connections to be made directly to the board itself. It is no longer necessary to attempt to match impedances on a part that is unchangeable, which allows for a 16 bit signal to be achieved at the output.

The new cryostat also allows for an incredibly large amount of scalability. This eliminates many design restraints when it comes to both the chip design and the PCB design for the next generations of IRSPs. The PCBs will no longer be constrained by size, which limits the chip design. Chips can become as large as possible as they will not be contained by a vacuum chamber, the chamber will accommodate the chips. By

sandwiching the PCB between two O-rings, the PCB itself becomes part of the vacuum chamber. It will hold a vacuum while not inhibiting board and chip growth.

Chapter 6

CONCLUSION

As the IRSPs advance, the demand for bigger and faster chips will continue to develop. The large-scale growth of the system, while driving progress, also brings its own set of challenges. Chiefly among them is the ever-present question of thermal management. Where the heat goes is a problem that plagues every modern system. In order to continue improving the SLEDs systems, this question must be answered in such a way that encourages future production as opposed to restricting it.

The currently available Dewar chambers are no longer satisfactory for previously discussed reasons and require a new type of Dewar. The new Dewar would be one that would solve the problems presented by the current packaging choice, namely heat removal, elimination of transmission lines, and scalability. By taking advantage of the PCB as a vacuum sealing wall, it becomes possible to solve the transmission and scalability problems. By partnering with *ARS Cryo*, it was possible to greatly solve the heat removal problem. These solutions will allow for the SLEDs systems to grow unhindered for many iterations to come.

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