OPTOELECTRONIC CHARACTERIZATION OF WIDE-BANDGAP $(AgCu)(InGa)Se_2$ THIN-FILM POLYCRYSTALLINE SOLAR CELLS INCLUDING THE ROLE OF THE INTRINSIC ZINC OXIDE LAYER

by

Uwadiae Obahiagbon

A thesis submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Computer Engineering

Fall 2014

OPTOELECTRONIC CHARACTERIZATION OF WIDE-BANDGAP $(AgCu)(InGa)Se_2$ THIN-FILM POLYCRYSTALLINE SOLAR CELLS INCLUDING THE ROLE OF THE INTRINSIC ZINC OXIDE LAYER

by

Uwadiae Obahiagbon

Approved: _____
Steven S. Hegedus, Ph.D.
Professor in charge of thesis on behalf of the Advisory Committee

Approved: _____
Kenneth E. Barner, Ph.D.
Chair of the Department of Electrical and Computer Engineering

Approved: _____
Babatunde Ogunnaike, Ph.D.
Dean of the College of Engineering

Approved: _____
James G. Richards, Ph.D.
Vice Provost for Graduate and Professional Education

ACKNOWLEDGMENTS

First and foremost, thanks to God for life and soundness of my mind and body to be able to complete this work and for His grace that has kept me going.

A heart-felt gratitude to Dr. Steve S. Hegedus for his guidance, advice, suggestions, questions and direction he provided through each step of this research work and for being a great source of encouragement even through the "darkest times" of my program. Your patience and dedication to educating the next generation is remarkable. I am also indeed very grateful to Dr. William N. Shafarman for your kindness and for taking a chance on me and also to Prof. Robert Birkmire for the opportunity to work at the IEC. I have learned a lot from the three of you through the interactions, questions, group meetings, and social events.

Thanks to Brian McCandles, Kevin Hart, Dr. James Mutitu, Christopher Thompson, Dr. JinWoo Lee, Lei Chen for your help with my experiments and for very useful academic and non-academic discussions and to Paula Newton and Sherry Stewart, it has been nice working with you and I will do it again. Go solar!

Thanks to my parents, Dr. & Dr. (Mrs) F. I. Obahiagbon for being true parents indeed and to my sibblings, Dr. Ikponmwonsa Obahiagbon, Dr. Osarobo Obahiagbon and Oy Obahiagbon, your love and prayers have kept me going.

Thank to my fiancée, Alzetta Clay, for your love, understanding and care and to Dr. Micheal A. Awaah and Dr. I. U. Awaah for their support and advice.

Thanks to the National Renewable Energy Lab (NREL) for providing funding for this research.

Finally, thanks to all my friends and to all staff and students of the institute of Energy Conversion and the Electrical and Computer Engineering, University of Delaware.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Experiments and simulations were conducted to vary the thickness and the sheet resistance of the high resistance (HR) ZnO layer in polycrystalline thin film (AgCu)(GaIn)Se_2 (ACIGS) solar cells. The effect of varying these parameters on the electric field distribution, depletion width and hence capacitance were studied by SCAPS simulation. Devices were then fabricated and characterized by a number of optoelectronic techniques.

Thin film CIGS has received a lot of attention, for its use as an absorber layer for thin film solar cells. However, the addition of Silver (Ag) to the CIGS alloy system increases the band gap as indicated from optical transmission measurements and thus higher open circuit voltage (V_{oc}) could be obtained. Furthermore, addition of Ag lowers the melting temperature of the alloy and it is expected that this lowers the defect densities in the absorber and thus leads to higher performance. Transient photocapacitance analysis on ACIGS devices shows sharper band edge indicating lower disorder than CIGS.

Presently there is a lack of fundamental knowledge relating film characteristics to device properties and performance. This is due to the fact that some features in the present solar cell structure have been optimized empirically. The goal of this research effort was to develop a fundamental and detailed understanding of the device operation as well as the loss mechanism(s) limiting these devices. Recombination mechanisms in finished ACIGS solar cell devices was studied using advanced admittance techniques (AS, DLCP, CV) to identify electronically active

defect state(s) and to study their impact on electronic properties and device performance. Analysis of various optoelectronic measurements of ACIGS solar cells provided useful feedback regarding the impact on device performance of the HR ZnO layer. It was found that thickness between 10-100 nm had negligible impact on performance but reducing the thickness to 0 nm resulted in huge variability in all device parameters. There was a weak improvement in all solar cell parameters with increasing HR layer resistivity by 3 orders of magnitude from 4E-3 to 1E1 Ω-cm. Additionally, optical characterization with ultraviolet-visible spectrophotometry (UV-VIS) and variable angle spectroscopic ellipsometry (VASE) of films, quantum efficiency (QE) of devices and modeling was used to perform a detailed optical loss analysis. .

Chapter 1

INTRODUCTION

1.1 Photovoltaic Cells and Solar Radiation

Research and development of solar cells have been ongoing for about 5 decades with the earliest work developed for space applications in the 60s. However solar cells for renewable energy applications started receiving attention in the mid-70s. A solar or photovoltaic (PV) cell is an electrical device that is capable of converting absorbed sunlight photons directly into electrons-hole pairs which constitutes the flow of current in a closed loop. The photon energy, E_{ph} is a function of wavelength, λ, and is related to the Planck's constant, h, and the speed of light, c, by

$$E_{ph} = \frac{hc}{\lambda} \tag{1.1}$$

Absorption will occur for photon energies greater than or equal to the bandgap, E_g (eV), of the semiconductor from which the solar cell is made; the amount of absorption depends on the thickness and absorption coefficient of the semiconductor. Fortunately, semiconductors presently used to make solar cell absorbers are favored by nature, as the peak emission radiated by the sun occurs in the visible region of the electromagnetic spectrum, with wavelength energies in the regime of a number of these semiconductors. The solar radiation reaching the earth suffers attenuation and scattering due to effects of the atmosphere (ozone, dust, air molecules, water vapor, etc.); however the solar irradiance reaching the earth amounts to 1000 W/m^2 on a clear sunny day. Terrestrial sunlight could vary widely in availability, intensity and spectral

composition [1] depending on atmospheric conditions, time of the day and time of the year but nevertheless, the amount of energy from the sun reaching the earth is enormous.

1.2 Power Conversion Efficiency and Theoretical Limits

A solar cell is a power generator capable of driving a load. The maximum power, P_{MP}, which the cell can deliver to an external load is given by

$$P_{MP} = V_{MP} J_{MP} \tag{1.2}$$

where V_{MP} and J_{MP} are the voltages and current density at maximum operating point as shown in figure 1.1.

The performance of a solar cell is characterized by the following parameters: short-circuit current density, J_{sc}, (mA/cm^2), open circuit voltage, V_{oc} (V) and FF and they are related to the power conversion efficiency, η, by

$$\eta = \frac{FF \times V_{oc} J_{sc}}{P_{in}} = \frac{V_{MP} J_{MP}}{P_{in}} \tag{1.3}$$

where P_{in} is the incident optical power determined from the light spectrum incident on the cell under test or connected to a load. Solar cell performance testing is carried out under standard test conditions (STC) for terrestrial applications which require:

1. The Air Mass 1.5 Global (AM1.5G) spectrum
2. Insolation of 1000 W/m^2 encompassing the spectral range from 200 – 2000 nm
3. And a device/junction temperature of 25 °C

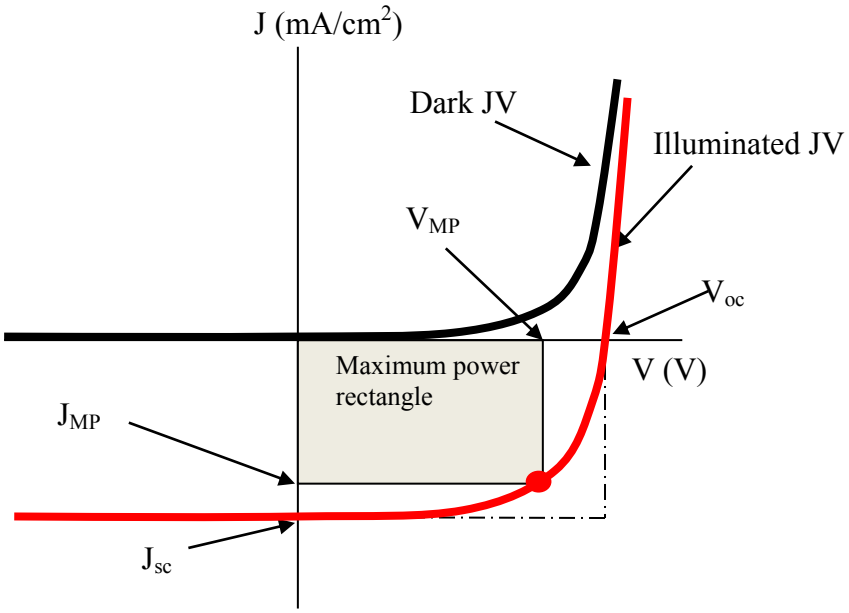


Figure 1.1: Current-voltage (JV) characteristics of a solar cell in the dark and under illumination.

Details of device operation and testing are presented in chapters 2 and 4.

Fundamentally, the largest losses in PV devices are losses due to thermalization for photons with energy, $E_{ph}>E_g$ and photons that are transmitted through the cells as they cannot be absorber, i.e., $E_{ph}<E_g$. For photons that lead to EHP generation ($E_{ph}=E_g$), in photovoltaic devices, additional limits like recombination of photo-generated EHPs, current and voltage losses due to design further reduces the performance of devices. Absorption of photons for the entire range of the solar spectrum will require more than one junction, or in other words, stacked semiconductor absorbers of different bandgaps (tandem solar cells). Under the Schockley-Queisser (SQ) theory [2] for single junction devices, with absorber bandgap, E_g, the optimum efficiency is achieved

for a bandgap range of 1.1 eV < E_g < 1.4 eV, with maximum conversion efficiencies around 33% [3].

Devices fabricated in this research effort are single junction devices with absorbers made from polycrystalline thin-film Silver Copper Indium Gallium Selenide [(AgCu)(InGa)Se_2] alloys commonly referred to as ACIGS, with bandgap ranging from 1.2 to 1.3 eV. Details of device structure and loss mechanisms are presented in chapter 2 and 4.

1.3 Thin-film Solar Cells

The need for alternative and renewable sources of energy has led to intensive research on solar cells over the past few decades. So far, ongoing research has explored several suitable material systems with the aim of producing low cost and high efficiency cells.

Solar cell absorber materials made from group I-III-VI semiconductors alloys are generally known as chalcopyrites. These material systems include Copper Indium diselenide (CIS), Copper Gallium diselenide (CGS) and Copper Indium Gallium diselenide (CIGS) and ACIGS. Other thin film technologies include Amorphous Silicon (a-Si), Cadmium Telluride (CdTe) and Copper Zinc Tin Selenide (CZTS). The laboratory efficiency of thin-film Cu(In,Ga)Se_2-based alloys has steadily increased over the years and hence it has received a lot of attention as a potential candidate for reducing the cost of module production. The present goal is to reduce the cost of module production to \$0.5/W_{peak} by 2020.

Presently, c-Si technology dominates the module manufacturing and installed PV arena contributing over 80% of all installed PV. The c-Si wafers are typically 180 – 220 μm thick. CIGS based solar cells allow much thinner absorber layers compared to c-Si technologies because of the high absorption coefficient of the Cu-chalcopyrites.

Thin films absorbers anywhere from 100nm to 4 μm have been fabricated using superstrate configuration [4] for submicron thicknesses and the standard substrate configuration [5] for relatively thicker absorbers. These materials are radiation-hard, cost-effective, and apparently immune to grain boundary defects [6, 7]. At the time of this writing researchers at ZSW have made small area (~1cm^2) $CuInGaSe_2$ (CIGS) based solar cells with a laboratory efficiency of 21.7% [10]. Previous record efficiencies of 19.9% [8], 20.3% [9] and 20.4% [11] have been reported. Thin film solar cells benefit from the use of smaller quantities of material reducing bulk material cost, hence production cost and module weight. Flexible CIGS thin films have also shown promising conversion efficiency, good stability, outdoor performance [12] and a high radiation resistance [13].

1.4 Objectives and Chapter Overview

In spite of the growth demonstrated by the CIGS-based solar cells, and despite the years of research, the material system and resulting device behavior is not completely understood. Little is known about the defect mechanisms controlling these devices. There is a relative difficulty (compared to c-Si) associated with extracting basic properties of the devices such as mobility, carrier concentration and doping profiles, defect distribution and energetic position of defects. The inability to directly and consistently measure these parameters limits the potential for a complete understanding of the path to improving laboratory devices. This has led to a greater difficulty in transferring laboratory technology to module production lines, hence hindering commercialization.

This research effort will focus on identifying, quantifying and separating the losses in ACIGS thin-film solar cells with the intent to elucidate the best opportunity for

improvement in device parameters in general, recommending potential modifications/optimization of the present device structure. Chapter 2 presents the device composition and standard device structure The ACIGS absorbers are deposited by co-evaporation using a baseline 3-stage process at the IEC.

Much effort in this thesis was focused on understanding the role of the high resistance/intrinsic ZnO (HR ZnO/i-ZnO) layer (discussed in end of chapters 2 and the whole of chapter 3). Experiments were conducted varying the thickness and the sheet resistance of the HR ZnO layer. The effect of varying these parameters on the optical properties of the film and device stack as well as the effects on built-in electric field distribution, depletion width and hence capacitance was studied on finished devices. Finished devices will be characterized by a suite of characterization techniques discussed in chapter 4, and these include: current-voltage measurements (JV), open circuit voltage vs. temperature (V_{oc}-T), quantum efficiency (QE), a host of admittance based techniques as well as analytical methods including diode analysis and optical loss breakdown. Multilayer simulation and measurements employing UV-VIS spectrophotometry, variable angle spectroscopic ellipsometry (VASE); and device simulation using SCAPS is presented in chapter 5. Details of devices results and loss analysis are presented in chapter 6.

Chapter 2

POLYCRYSTALLINE CHALCOPYRITE THIN FILM CIGS-BASED SOLAR CELLS

In this chapter, the behavior of the CIGS alloy systems with respect to composition will be covered. The standard device stack, the method of fabrication and role of each layer in the stack is explained. Experiments to optimize the ZnO layer are introduced and specific effects due to Ag alloying of CIGS absorbers are discussed. The chapter ends with a simple explanation of the device operation in general.

2.1 Copper Indium Gallium Diselenide Solar Cells (CIGS)

Solar cells fabricated from the quaternary alloy $CuIn_{1-x}Ga_xSe_2$ have emerged as one of the most promising thin film technologies. Copper chalcopyrites of the general composition $Cu(InGa)(Se)_2$ offer a wide range of bandgap from 1.02 eV for $CuInSe_2$ to 1.68 eV for $CuGaS_2$ [7]. Laboratory solar cells and commercial solar modules with high efficiencies are prepared from material of certain composition made possible by the ability to substitute Ga for In atoms in the $CuInSe_2$ system forming the $CuIn_{1-x}Ga_xSe_2$ alloy. The bandgap is controlled by the amount of Ga in the film.

$$x = \frac{Ga}{[Ga + In]} \tag{2.1}$$

Highest performing devices have a Ga/(In+Ga) ratio of 25 - 30% [5, 7] corresponding to a bandgap of approximately 1.2eV or less. Several growth methods and recipes have been explored and some techniques and features like bandgap gradients are used to improve operating voltage and current collection [69]. Overall, CIGS is a referred to

as a very forgiving material system as high performing devices have been fabricated from wide range of group I and group III elemental composition. For example, solar cells with high performance can be fabricated with copper ratio, Cu/(In+Ga) of 70 - 90% [5, 14].

2.2 Device Structure and Fabrication/Deposition Methods

The schematic in figure 2.1 is a typical CIGS/CdS thin-film PV device. In this design, the device is fabricated on a Mo coated glass, metal, or polymer substrate. The typical substrate used for these cells is Mo coated soda-lime glass. It is widely accepted that Na out-diffusion from the soda-lime glass (SLG) during absorber growth beneficial for device performance, although the exact mechanism behind this increase in photovoltaic properties is not well understood. The exact role of sodium in CIGS solar cells has been debated with no agreement in the literature. While some researchers propose that Na diffusion from the glass into the absorber layer reduces defects and enhances photovoltaic properties [7, 15], and that Na replaces the In_{Cu} antisite defects, reducing the density of compensating donors and also increases the net acceptor density [15, 16], other researchers have found that Na played no significant role in device operation or performance, fabricating high efficiency devices on sodium-free substrates with and without post deposition of sodium.

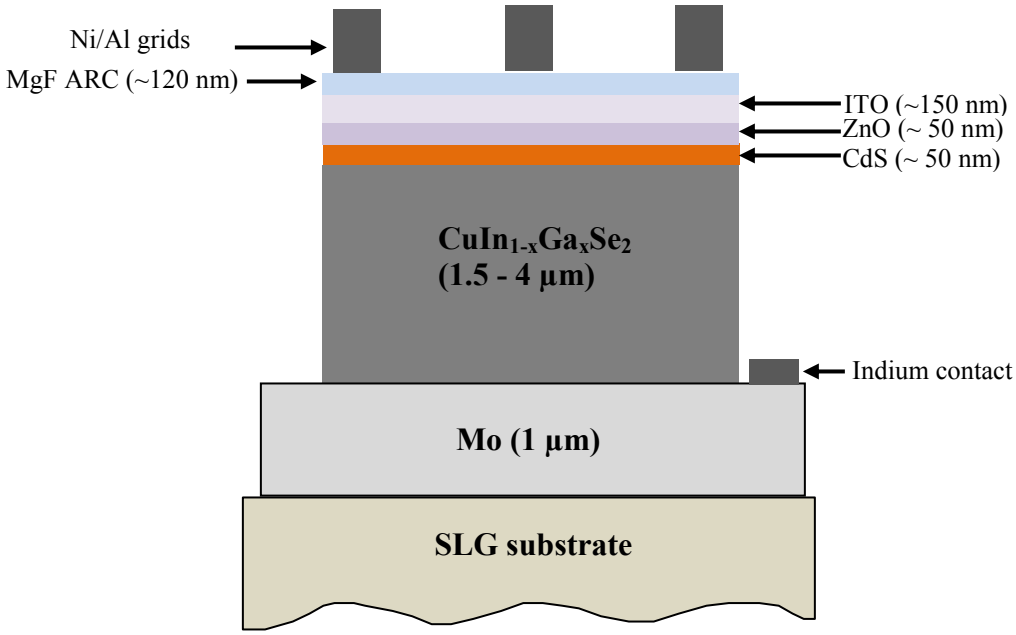


Figure 2.1: Schematic of a conventional $CuIn_{1-x}Ga_xSe_2$ solar cell structure

2.2.1 Absorber layer deposition

Copper indium gallium diselenide films grown on soda lime glass are typically large grain polycrystalline with a columnar structure and a high aspect ratio [7]. The absorbers used in this research are deposited by multi-source co-evaporation process in a selenium rich atmosphere making the material p-type. Other methods of CIGS absorber preparation have been employed in laboratory as well as module applications. These methods include selenization of metal precusors [17] and rapid thermal processing of stacked elemental layers deposited by sputtering.

The elemental source bottle configuration is shown in figure 2.2.

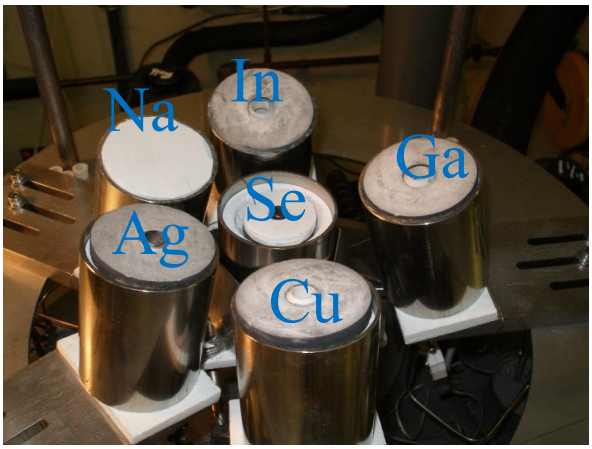


Figure 2.2: Source configuration in belljar evaporator

The Belljar system used has a substrate holder capable of holding 9 pieces of 1x1 inch Mo-coated SLG substrates. The substrates are suspended over the elemental sources, such that when the source bottles are heated beyond the melting point of the metals, metal vapors rise from the sources toward the substrate and are deposited onto the substrate. It is common to control the temperature and time cycle of the sources and the substrates during deposition to achieve specific alloy compositions and gradients. The substrates are typically heated to a maximum temperature of 580 °C toward the end of the growth process. The deposition process involves an initial deposition of In and Ga in a Se rich atmosphere followed by a Cu deposition followed by In and Ga deposition, a process referred to as the Boeing process [18]. The recipe used here is the so called three-stage process after Gabor et al. [19]. Although slight modifications have been made to the original process the temperature profile and activity in all stages is as shown in figure 2.3.

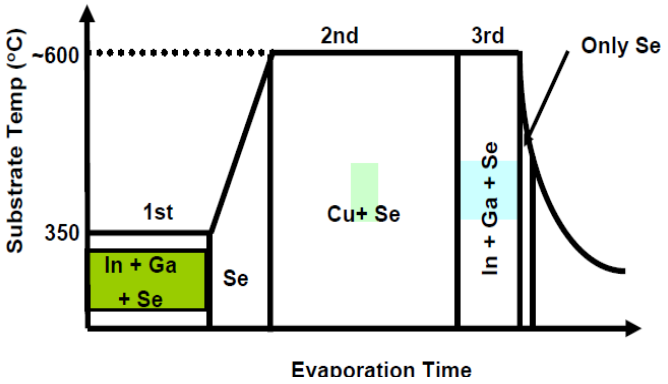


Figure 2.3: Substrate temperature profile and elements deposited in three-stage process.

In the first stage $(InGa)_2Se_3$ is deposited with the substrate at 350 °C with the Cu source in idle mode, the length of the deposition is determined by the intended thickness. For 2 µm thick films, the first stage lasts for about 20 min. Prior to the second stage the substrate temperature is ramped up to 580 °C, while depositing Cu and Se keeping the other sources at idle temperatures or shuttered off. During the second stage the film is driven to a Cu rich composition and the end point detection is by a thermocouple embedded in one of the substrates. The Cu-rich point is detected by a change in emissivity of the film, characterized by an increase in reflected heat from the samples, causing them to cool down slightly. An embedded thermocouple behind one of the substrates is used to track the substrate temperature. When this temperature decreases, the PID controller supplies more heat, by increasing the power supplied to the substrate heater. The heat supplied from the substrate heater is sensed by a floating thermocouple lying between the heater and the substrates. The floating thermocouple temperature is monitored for a temperature spike in an otherwise flat/steady temperature profile. The third stage involves the deposition of In, Ga and Se to

produce a final film which is In rich although the film was Cu rich at the end of the second stage. For a 2 μm thick film the second stage lasts for 30 min while the third stage could be anywhere from 16 to 23 min depending on the amount of In, Ga required to make the film stoichiometric. The deposition termination is followed by a 10 - 15 min anneal in Se atmosphere and interdiffusion between the elements from the various stages form a uniform film. Higher (up to 650 °C) and lower temperatures (450 °C) have been implemented in the second and third stages with no consistently significant benefit in terms of device results reported at this time. Although it is assumed that deposition at higher temperatures may lead to higher quality absorber layers, due to large grain structure, higher deposition temperatures also tend to increase impurity incorporation into the films and is a significant increase in thermal budget on a production scale. A more detailed description of the 3-stage process by Shafarman et al is found in chapter 13 of [5].

As-deposited CIGS films are large grain (~1 μm), figure 2.4, polycrystalline in nature with benign grain boundary defects and a columnar structure [20].

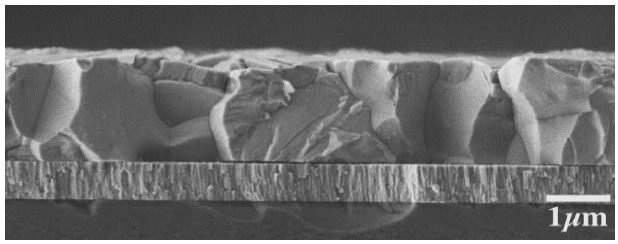


Figure 2.4: SEM cross-section of an ACIGS film grown at 580 °C

Although Mo contact on CIGS material is rectifying, during film growth an interfacial layer of 10 – 30 nm $MoSe_2$ is formed between the Mo and the absorber which provides a suitable ohmic contact to the device.

2.2.2 Junction formation

A 50 nm thick CdS layer showed in figure 2.1 forms the n-side of the junction with the p-type absorber. This has been the norm from earliest research with CIS during which time the CdS layer followed by a 1 μm thick Indium doped CdS window layer were both deposited by vacuum evaporation [21]. Details of the evolution of the window layer structures are presented briefly in Chapter 3. The CdS layer now is typically deposited by chemical bath deposition (CBD) also referred to as solution growth process. The bath is alkaline with a pH > 9 and consists of three compounds: a cadmium salt (e.g. cadmium sulphate, $CdSO_4$), a complexing agent, (usually ammonia, NH_3) and a sulphur precursor (thiourea, $SC(NH_2)_2$). The substrate consisting of the absorber deposited on Mo-coated SLG is immersed in the chemical bath immersed in a water bath and heated up to 60 – 80 °C by a hot plate. A magnetic stirrer is used to ensure uniformity of the solution and a thermocouple used to monitor the temperature. A dense homogenous film grows on the absorber by an ion-by-ion reaction or a clustering of colloidal particles [5]. The CdS bath conditions especially the presence of NH_3 helps to reduce recombination at the interface by chemically etching/cleaning the surface of the absorber enabling epitaxial growth of the CdS layer. The CdS CBD deposition also helps match the lattices of the window and absorber. A lot of effort has been put into alternate buffer layers as well as deposition methods suitable for large scale production aside the fact there is still a considerable debate on the exact chemistry of the interface between CdS and CIGS.

2.2.3 Window layer and top contact deposition

The transparent conductor (TCO) on the top of the cell structure shown in figure 2.1, is usually made from Al-doped ZnO (AZO) or Indium Tin Oxide (ITO) which are both transparent conductors, with AZO slightly favored for large scale production because of its cost advantage over ITO. The ZnO window is doped with Al to reduce the lateral sheet and contact resistances. The current must flow laterally through the TCO to the grids for collection. The i-ZnO and the TCO layer are deposited by sputtering from ceramic targets in an Ar/O_2 ambient depending on the properties desired.

2.2.3.1 Deposition of the high resistance (HR) ZnO (i-ZnO) window layer

The HR ZnO layer (discussed in chapter 3) is deposited by rf sputtering from an intrinsic ZnO target in a CVC sputtering system. Experiments were conducted with an attempt to vary the thickness and the sheet resistance of the HR ZnO layer. The effect of varying these parameters on the electric field distribution across the device, depletion width and hence capacitance were studied by simulations presented in chapter 5. Devices were then fabricated and tested with the results are presented in chapter 6.

The traditional 50 nm i-ZnO was used as control in both the thickness and sheet resistance experiments.

2.2.3.1.1 HR ZnO thickness variation

Intrinsic ZnO layers were deposited by rf sputtering. The sputtering chamber was pumped down to a base pressure of ~1.5E-6 Torr and then an Ar based plasma is used to sputter the ZnO from the target at a deposition pressure of ~5 mT/Ar with no oxygen added and Ar gas pressure set at 28 sccm. The rf power was 700 W and a pre-

deposition of 5 min was used to sputter off surface contaminants from the target. The sheet resistance of the deposited film was >1 MΩ/□. The thickness of the films was changed by varying the deposition time keeping the growth rate constant at ~8.3 nm per min. The i-ZnO thickness ranged from 0 to 100 nm.

2.2.3.1.2 ZnO Sheet resistance variation

The goal here was to change the sheet resistance of the i-ZnO layer only, in the standard cell structure. The i-ZnO films from undoped target discussed above represented the high end of the resistivity range. To obtain lower resistivity, an Al-doped ZnO ceramic target (AZO) was used. The sheet resistance was changed by the amount of O_2 introduced during the sputtering process as presented in table 2.1.

In all cases, the thickness of the AZO was maintained at 50 nm and was followed by the standard ITO layer deposition. The sputtering is similar to that presented above except that an AZO target is used with a dc power source and the deposition conditions are slightly varied to achieve the desired properties as detailed in table 2.1

Table 2.1: Sputtering parameters for sheet resistance experiments with AZO

Base pressure (Torr)	1.6E-6	1.6E-6	1.6E-6
Ar (sccm)	50	12	0
Ar/O_2 (sccm)	0	38	50
Percent of O_2	0	1.52	2
DC power (W)	80	80	80
Pre-deposition time (min)	30	60	60
Deposition time (min)	6	6	6
Thickness (nm)	50	50	50
Sheet resistance, R_{sh} (Ω/□)	700	35 K	138 K

The sheet resistance was varied by an order of magnitude for three samples and a control sample from the same absorber run having a HR ZnO layer was also referenced.

2.2.3.2 Transparent conductor, metal grids and anti-reflection coating (ARC)

Cells made at the IEC use an ITO transparent TCO. The window layer refers to the i-ZnO/TCO combination. The functions of the TCO are twofold: (a) to allow sunlight enter the cell and be absorbed (b) to act as a top contact to efficiently collect charged carriers that have been separated by the p-n junction. Hence this layer has a high lateral conductivity

ITO was deposited by rf sputtering at a power of 700 W at an Ar/O_2 mixture with 0.88% O_2 for 10 min preceded by a 30 min pre-deposition. A typical thickness of 150 nm was obtained for the very conductive ITO layer. The standard ITO thickness was maintained for all cells fabricated for both the thickness and sheet resistance experiments and cells in each group received the ITO deposition in one pass, in the same run to eliminate run-to-run variations of the ITO process. The sheet resistance of the ITO is typically between 20 – 50 Ω/□.

Electrical contact is made to the front of the device via metal grids deposited on the TCO. The grid design is optimized after [1] to minimize grid shadowing and power losses due to resistance. The top contact consists of a few nanometers of Ni deposited by e-beam evaporation through a mask followed by Al giving a combined metal grid thickness of 1 μm. The purpose of the thin Ni layer is to prevent the formation of a high-resistance oxide layer [5]. The mask has four cells outline on the top surface. On each 1x1 inch substrate, two 1 cm^2 and two 0.4 cm^2 cells are delineated by scribing

using a diamond carbide scribe. The scribing isolates each individual cell for electrical measurements.

2.3 Silver Copper Indium Gallium Diselenide (ACIGS)

In the past decade a considerable effort has been put into research on the role of Ag alloying in the CIGS system. Most of this effort toward Ag alloying has been done at the IEC. The most efficient devices made till date is 18.5% certified by NREL. Cu atoms are substituted by adding small amounts of Ag during the 3-stage growth process. The deposition process is essentially the same as detailed in section 2.3.1 except that a silver source is added as shown in figure 2.2. The Ag profile follows the Cu profile during the deposition as shown in figure 2.5.

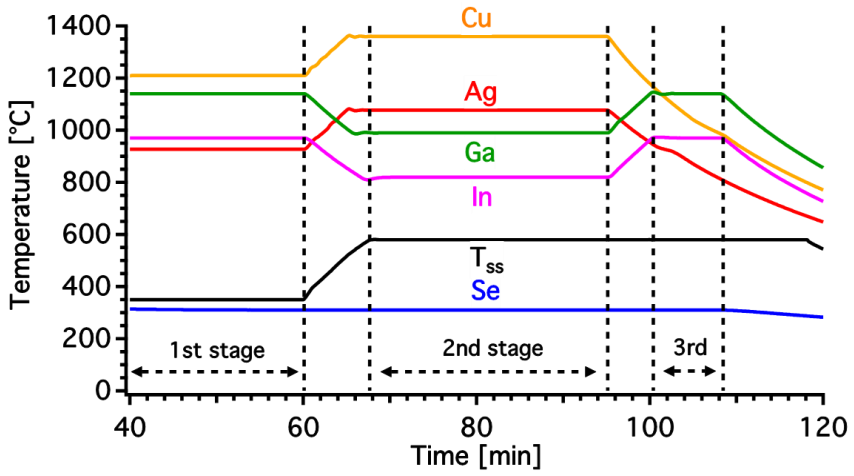


Figure 2.5: Temperature profile for 3-stage co-evaporation of ACIGS showing substrate temperature profile (T_{SS}) and elemental source profiles.

Alloying with Ag provides yet another means of tuning the bandgap of the alloy system based on Ga/(Ga+In) and Ag/(Ag+Cu). Ag varies the bandgap slightly up to a 0.2 eV change for a given Ga/(Ga+In) composition as shown in figure 2.6 below.

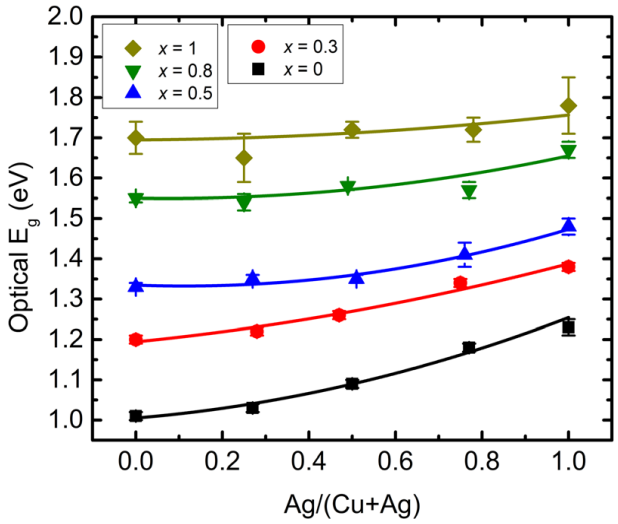


Figure 2.6: Bandgap change with Ag addition for a fixed Ga/(In+Ga) ratio [22]

The lower melting temperature of the ACIGS alloy compared to the CIGS alloy suggests that Ag may allow the formation of absorber layers with lower disorder. Transient photocapacitance (TPC) shows a steeper exponential band tail compared to CIGS as depicted in figure 2.7, consistent with less disorder [23, 24].

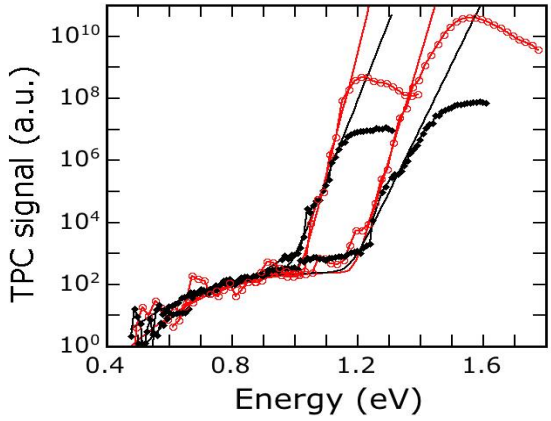


Figure 2.7: Transient photocapacitance spectra for ACIGS (red) and CIGS (black) [23].

Free carrier density as measured by drive level capacitance profiling (DLCP) indicates relatively lower free carrier density in ACIGS 3 stage devices compared to CIGS devices. The details of DLCP measurements is presented in chapter 4 and the effect of low carrier density on device parameters and performance is studied by simulation and presented in chapter 5. The effect of low carrier density on ACIGS device performance is yet to be understood. However at the time of this writing, the ACIGS alloys produced at the IEC yield higher device performance compared to CIGS devices produced by the same process.

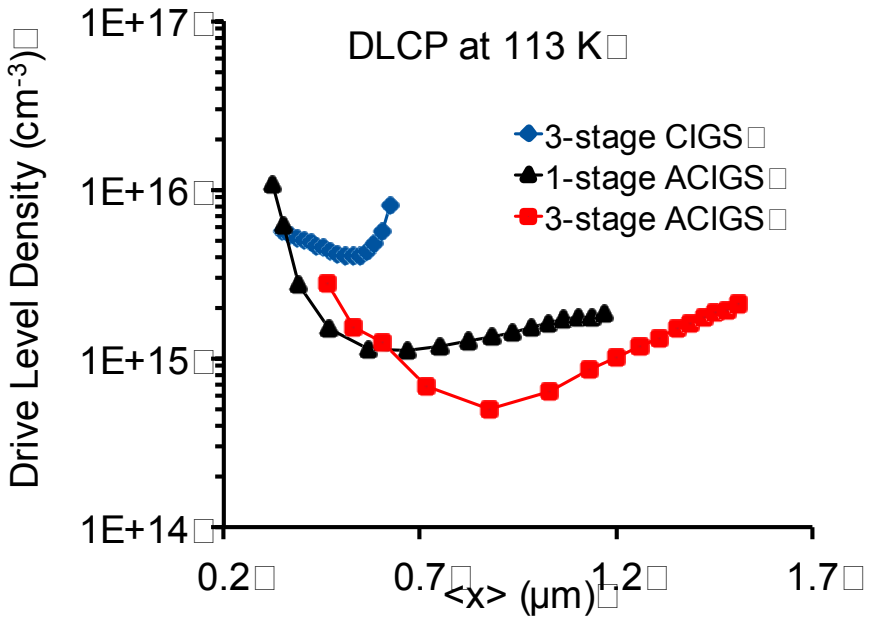


Figure 2.8: Drive level capacitance profiling of ACIGS vs. CIGS fabricated at IEC

Significant effort is ongoing to optimize the 3-stage process for ACIGS as well as optimizing the device structure including alternate window and buffer layers minimizing optical and voltage losses.

Chapter 3

THE ROLE OF HIGH RESISTANCE ZINC OXIDE (i-ZnO) IN ACIGS DEVICES

As mentioned in chapter 2, substitution of In with Ga [25], led to the so called Boeing Process in CIS solar cells. Independent of this development, a substantial decrease in the CdS layer thickness from about 2 μm to 50 nm [26] with an accompanying 50 nm thick i-ZnO window layer was accepted as the norm. Significant improvements in photocurrent resulted, as the absorption in the blue region by the thick CdS layer was reduced [27, 28]. Being a wide bandgap material (~3.4 eV) with a refractive index less that the CGS and CIS, the role of the i-ZnO layer was thought to be twofold: (1) the improved transparency of the i-ZnO/CdS combination, permitted increased photon harvesting in the short wavelength region (360 – 520 nm); (2) i-ZnO with a refractive index of 2, acts as an antireflection coating. The modified solar cell structure (i-ZnO/CdS/CIGS) was quickly adopted and has essentially stayed the same. Presently, the i-ZnO thickness and electronic properties has been standardized. However, it is nearly universally found that the success of this front widow stack requires a high resistivity ZnO layer of thickness ~50 nm situated between the 50 nm thick CdS and a 150 nm thick ITO or Al:ZnO (AZO) transparent contact/window layer.

The exact role of the intrinsic ZnO layer has been a question of debate since and several models have been proposed to explain its function. While high

performance devices have been made without the ZnO layer some researchers have reported degradation of device parameters when the ZnO layer was omitted.

The goal of this chapter is to review the literature and document previous work investigating the role of the HR ZnO layer, with emphasis on the effect of this layer on device parameters. Results of experiments with thickness and sheet resistance of the ZnO layer at the IEC is presented in chapter 6.

3.1 Window and Buffer Layers Definitions

The standard CIGS based solar cell structure in use today consists of a CdS buffer layer and a window layer consisting of a thin HR ZnO (i-ZnO) and a thicker AZO or ITO layer. In this thesis, window layer will refer to the i-ZnO/ITO or i-ZnO/AZO combination, the buffer layer refers to the CdS layer only, while transparent contact (TCO), refers to the conductive AZO or ITO layer only. The resistivity of the TCO could range between 10^{-4} – 10^{-3} Ω cm depending on method of deposition [5]. The sheet resistance, R_{sh}, is expressed as

$$R_{sheet} = \frac{\rho}{t} \tag{3.1}$$

where *t,* is the thickness of the thin film.

3.2 Electronic and Optical Properties of HR ZnO

The HR ZnO is typically deposited by rf magnetron sputtering from a ceramic intrinsic zinc oxide target. Other methods for large scale production including reactive sputtering, have been explored to reduce cycle time and effective processing cost. Depending on the deposition method, the resistivity, ρ, of the layer could range between 1 – 100 Ω cm [5]. A high resistance ZnO film deposited under conditions used in the baseline ACIGS solar cells at the IEC is typical 50 nm thick, with an ~80%

transmission in the visible region including some absorption from the glass substrate as shown in figure 3.

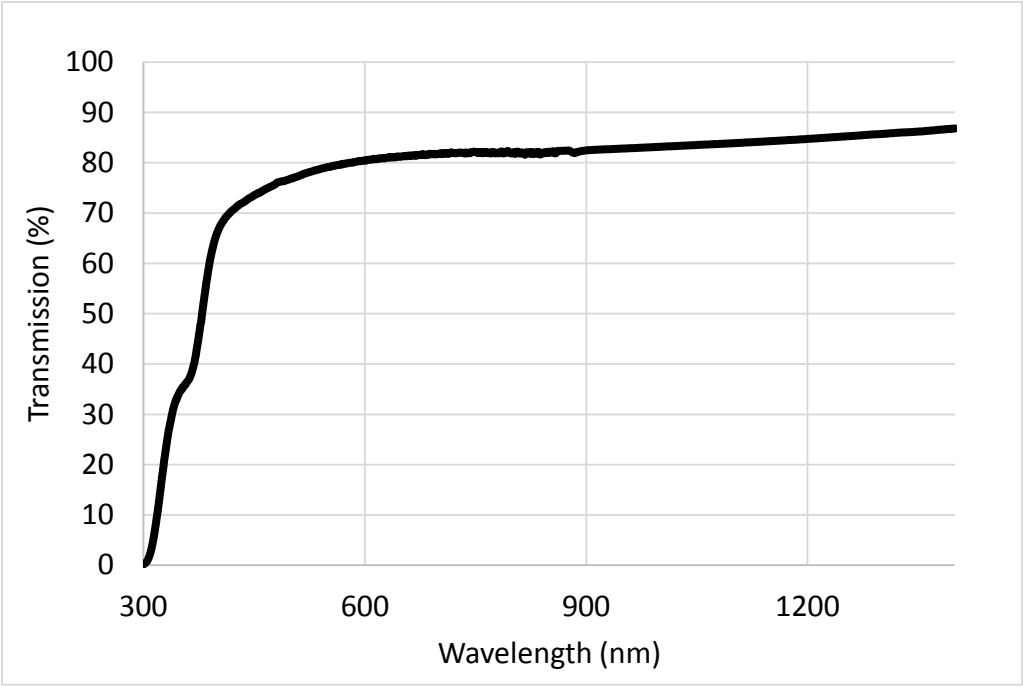


Figure 3.1: Transmission of a 50 nm thick ZnO film deposited on glass. Films sheet resistance is in the MΩ/□ range.

3.3 Effect of Varying i-ZnO Thickness

In standard CIGS-based solar cell structures the thickness of the i-ZnO layer tends to be around 50 nm. Several studies has been conducted to investigate the effect of the thickness with a view to optimize the required thickness and device performance. It would seem as though the effect of thickness cannot be considered independent of the CdS layer. The surface of as-deposited absorber layer films by co-evaporation at the IEC have been reported to have RMS roughness of ~50 – 100 nm

[29] measured by AFM before KCN or Br etch. While some researchers believe that the i-ZnO plays no significant role in the device. Others propose that the conformal 50 nm CdS layer deposited by CBD could thus have thin spots leading to 'weak diodes' or pin holes. This is where the ZnO comes in.

Kessler et al reported that the i-ZnO layer may be unnecessary if the CdS is sufficiently thick. In this work, the ZnO layer was deposited by rf magnetron sputtering [30] and the CdS thickness was increased by increasing the CBD deposition time. Devices with and without i-ZnO were deposited and processed in pairs for several CdS thickness as shown in figure 3.2. The results suggest that the presence or absence of i-ZnO layer did not matter as long as the CdS was thick enough.

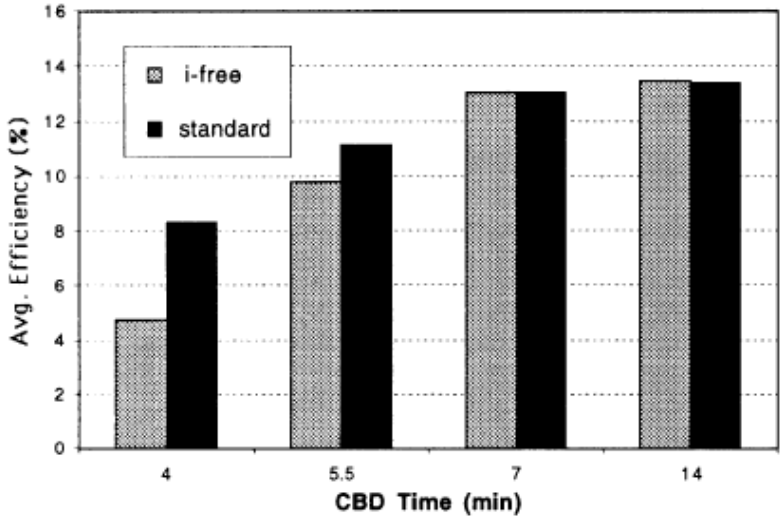


Figure 3.2: Device efficiencies obtained as a function of CBD (CdS) time (i.e. CdS thickness) for the standard and the i-ZnO free devices [20, 31]

Rau et al after a series of experiments [32] referred to the function of the i-ZnO layer as "a mystery" and concluded that the combination of CdS and i-ZnO prevents electrical inhomogeneity across the junction from dominating the open circuit voltage of the entire device.

Ruckh et al explored the performance of devices with various i-ZnO thicknesses. They report that the i-ZnO layer thickness was uncritical for device performance [33] and their findings are shown in Table 3.1

Table 3.1: Device properties of cells with i-ZnO of different thickness [33]

thickness of i-ZnO (nm)	V_{oc} (mV)	FF (%)
0	620	74
25	621	75
250	628	74

Hasoon et al eliminated the CdS layer completely conducting two experiments in which they deposited the i-ZnO layer directly onto the absorber as-deposited and after the absorber was etched with NH_4OH [34]. ZnO was deposited by MOCVD. Although they report an increase in device efficiency for Cd-free devices after heat treatment, they also observe a significant decrease in V_{oc}. Etched samples did not yield better results.

Scheer et al examined laboratory scale modules [35], studying the role of the i-ZnO layer by preparing samples of varying thickness from 0 to 210 nm. They report that the effect of i-ZnO on V_{oc} is not systematically observed, although at higher thickness, distribution of V_{oc} becomes smaller and that the effect of i-ZnO on J_{sc} as thickness increases is observed due to optical absorption as shown in figure 3.3. They

conclude that the effect on cell performance is negligible as long as the i-ZnO thickness is below 100 nm as is usually the case in standard device structures and suggest that the role of the i-ZnO layer is to reduce the impact of randomly occurring shunt paths in devices.

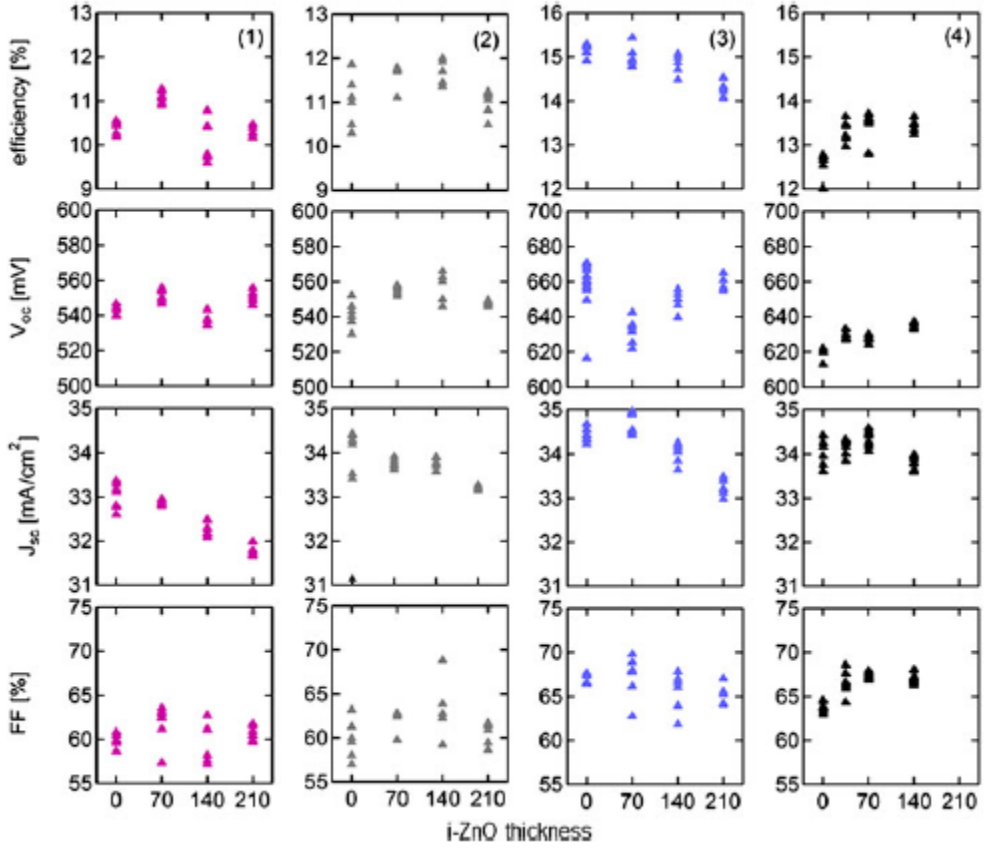


Figure 3.3: Solar cell parameters for module cells as a function of i-ZnO thickness for four different device process series (0, 70, 140 and 210 nm thick i-ZnO) [35]

From the figure 3.3, the authors propose that the presence of the i-ZnO leads to a somewhat smaller spread of device parameters in the presence of randomly occurring

shunts in the device. In the absence of shunt paths, the device parameters of cells and modules without i-ZnO are similar to those with a thin layer of i-ZnO. That is, in an ideal device, the i-ZnO will not be necessary.

Other researchers [36, 37] have reported that generally, there was no significant influence of the i-ZnO processes on device performance and that omitting the i-ZnO layer had no effect on efficiency. Studies on module stability may however suggest that the i-ZnO layer is necessary [36].

3.4 Effect of Varying i-ZnO Resistivity

Although not much work on the effect of directly varying the sheet resistance of the i-ZnO could be found reported in literature, there has been no agreement in the literature regarding the exact role of resistivity of the i-ZnO layer, keeping in mind that the sheet resistance is a function of thickness.

Ruckh et al varied the resistivity of the i-ZnO layer by adding O_2 during the sputtering process [33]. Figure 3.4 shows the device results. They conclude that the addition of O_2 had no effect on device performance.

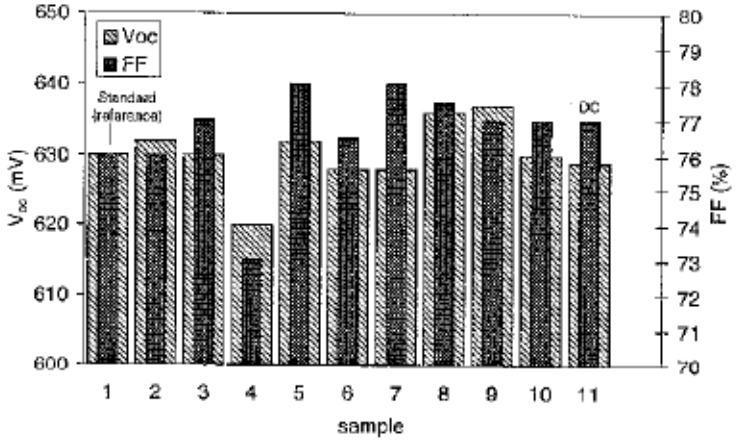


Figure 3.4: Device properties of solar cells with different i-ZnO obtained by varying the oxygen flow during the sputtering process [33]

3.5 Importance of ZnO in CIGS-based Devices

In summary, the exact role of the i-ZnO layer may remain an open question for researchers. Results of experiments at the IEC are presented in Chapter 6, where effects of varying the thickness as well as the sheet resistance of the i-ZnO layer are reported.

Overall, it would appear that there is a benefit to using the i-ZnO layer rather than a detriment. However eliminating this layer successfully will be a cost saving in module production. The continued presence of this layer may be tied to the use of a thin CdS buffer layer in standard structures, hence successful development of alternative buffer layers like Zn(S, O, OH) may eventually mark the end of the i-ZnO era. At the time of this writing, it is believed that the role of the i-ZnO layer is not unrelated to reducing the effects of non-ideal spatial uniformity which may include pin holes and weak spots as well as serving to protect the CIGS/CdS junction from subsequently harsh processing steps. Most of the standard structure for CIGS-based

solar cells has been adopted for ACIGS solar cell structure. It would be interesting to find out how much change and flexibility Ag alloying provides in the future.

Finally, the i-ZnO layer has been shown to be critical in improving the absolute performance and reducing the variability in performance for CdTe thin film devices. In particular it improves the Voc as CdS thickness decreases thus enabling higher Jsc without losing Voc. A range of materials have been studied as HR window bilayer. Its role has been identified as blocking weak barriers or shunts from dominating the Voc [38]. It is possible that the i-ZnO in CIGS technology may be most beneficial at the module level where large area uniformity is crucial. It may increase the homogeneity of the buffer/absorber or buffer/window junction.

Chapter 4

OPTOELECTRONIC CHARACTERIZATION OF THIN FILM SOLAR CELLS

In this chapter, techniques to determine the characteristic response of fabricated ACIGS solar cell are detailed. The characterization techniques explored here will typically employ the use of an optical (full spectrum or monochromatic) or electrical (ac or dc) excitation of some sort. Device characterization is extremely important for understanding device behavior and limiting mechanisms, with a view to improve the overall device performance. The overall goal is couple device results with process variables providing useful feedback for improvements in device design, processing and optimization. This is very important for thin film devices as a consensus has not been reached (at the time of this writing) regarding certain observed phenomena including metastabilities, grain boundaries and the defect physics of this class of devices. The following characterization techniques were used to analyze films and finished devices and the measurement systems are also briefly described: current/voltage (JV) analysis, quantum efficiency (QE), Mott-Schottky capacitance-voltage (CV), drive level capacitance profiling (DLCP), admittance spectroscopy (AS), ultraviolet-visible spectrophotometry (UV-VIS), variable angle spectroscopic ellipsometry (VASE), and electroluminescence (EL).

4.1 Current-voltage (JV) Characteristics

The current-voltage sweep (JV) is the most fundamental measurements made on a solar cell [3]. The method consists of a four-point measurement system where the

current of a solar is measured as a function of applied voltage in the dark and under illumination. The most important performance metrics of the solar cell including the efficiency are derived from the JV sweep. The measurements were performed under Standard Test Conditions (STC), AM1.5G spectrum, 100 mW/cm^2 insolation, and junction temperature of 25° C. An OAI Solar Class AAA Simulator having a Xenon filtered lamp was used for the illumination source. Before measurement the light source is calibrated using standard silicon cells measured at the National Renewable Energy Laboratory (NREL). The cell is mounted on a temperature controlled stage (regulated by a chiller) and contacted using a set of Kelvin probes. The four-point or Kelvin probe method ensures that parasitic resistance effects due to connecting wires (R_w) and contact (R_c) to the device, does not contribute to the measured values of V and I. The high input impedance (R_m) of a voltmeter (10^{12} Ω or higher) ensures that little or no current flows through the voltage path [39] as shown in Fig 4.1 below.

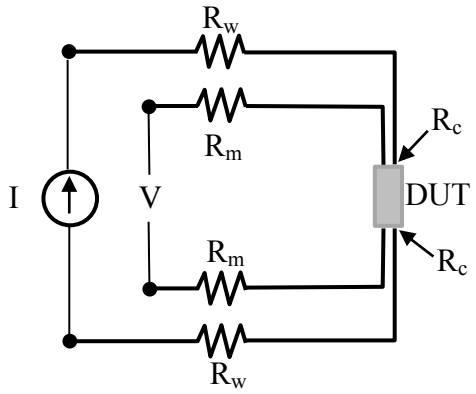


Figure 4.1: Schematic Kelvin prove set up for JV measurements

Hence voltage is applied by a set of probes and current is measured by another set of probes such that all points in the circuit are at an equipotential and hence there is

no voltage drop in the loop. A Keithley source-measurement unit (SMU) Model 2400 serves as the voltage source and current measuring unit.

The following parameters are of utmost interest for any solar cell: a plot of JV in the dark and under illumination, where the short circuit current density, J_{sc} (mA/cm^2), open circuit voltage, V_{oc} (V), fill Factor, FF and power conversion efficiency, η are determined from the illuminated curve.

4.1.1 Diode analysis

A solar cell is p-n junction and the ACIGS/CdS is an example of a heterojunction. The metallurgical junction formed between the absorber and CdS sets up a built-in electric field in the solar cell. The CdS is highly doped allowing for the transport of carriers through the device. Where J_0 is the reverse saturation current that is determined by the dominant recombination mechanism in the device, q is the elementary charge, V is the applied voltage bias, k is the Boltzmann's constant and T is the temperature [40], the ideal solar cell equation can be expressed as

$$J = J_0\left(e^{qV/kT} - 1\right) - J_L \tag{4.1}$$

Equation 4.1 is an extension of equation 2.2 in chapter 2. Equation 4.1 incorporates the ideality factor which describes the dominant recombination mechanism in the cell and also includes parasitic effects, namely series and shunt resistance.

$$\mathrm{J} = \mathrm{J}_0 \exp\left[\frac{q}{n_{id}KT}(V - R_s J)\right] + GV - J_L \tag{4.2}$$

The parameters V_{oc}, J_{sc} and FF obtained from JV measurement analysis are well accepted indicators for the performance of solar cells. Even more information could be obtained by careful examination of the JV curves and performing basic mathematical

operations on the solar cell diode equation. This procedure enables the extraction of series resistance, R_s (Ω/cm^2), shunt conductance, G (S/cm^2) or shunt resistance, r_{sh} (Ω/cm^2), diode ideality factor n_{id}, and diode saturation current J_0 (mA/cm^2). Details of this analysis can be found elsewhere [41] but in summary the following steps are followed:

For $k = 8.62 \times 10^{-5}$ eV/K; $q = 1.6 \times 10^{-19}$ C; T = 298 K

1. Plot dark and light J (mA/cm^2) vs. V (V)
2. Plot dJ/dV (mS/cm^2) vs. V (V) for the dark curve.

   Determine the shunt conductance from G (mS/cm^2) from the value of the dJ/dV near $J_{sc.}$ This gives G, the shunt conductance (or shunt resistance, Rsh = 1/G). Shunt resistance should be as high as possible for a good solar cell.
3. Plot dV/dJ ($\Omega.cm^2$) vs. $(J+J_{sc}-GV)^{-1}$ ($mA^{-1}.cm^2$).

   Determine n_{id} from slope ($S = n_{id}kT/q$) and R_s (Ω-cm^2) from y-intercept for both dark and light curves. $J_{sc} = 0$ for dark curve, GV = 0, if shunt resistance is very high, so that GV is very small/negligible.
4. Plot semilog of $(J+J_{sc}-GV)$ (mA/cm^2) vs. $(V - R_sJ)$ (V).

   Determine J_0 (mA/cm^2) from y-intercept and n_{id} from slope ($S = q/n_{id}KT$). Plot for both dark and light JV curves and compare n_{id} with values obtained from (3). $R_s = 0$, GV = 0, if negligible.

   The shunt conductance and series resistance are parasitic effects due to geometry and bulk properties, they contribute to power loss in the device. Correcting for the shunt conductance by subtracting GV from $J+J_{sc}$ and removes the effect of the current contribution due to shunts in the device. To

correct for the voltage drop across the series resistance, JR_s is subtracted from V. The actual bias across the junction is (V – JRs).

A representative output of the 4 steps in the analysis described above is shown in the Figure 4.2 below:

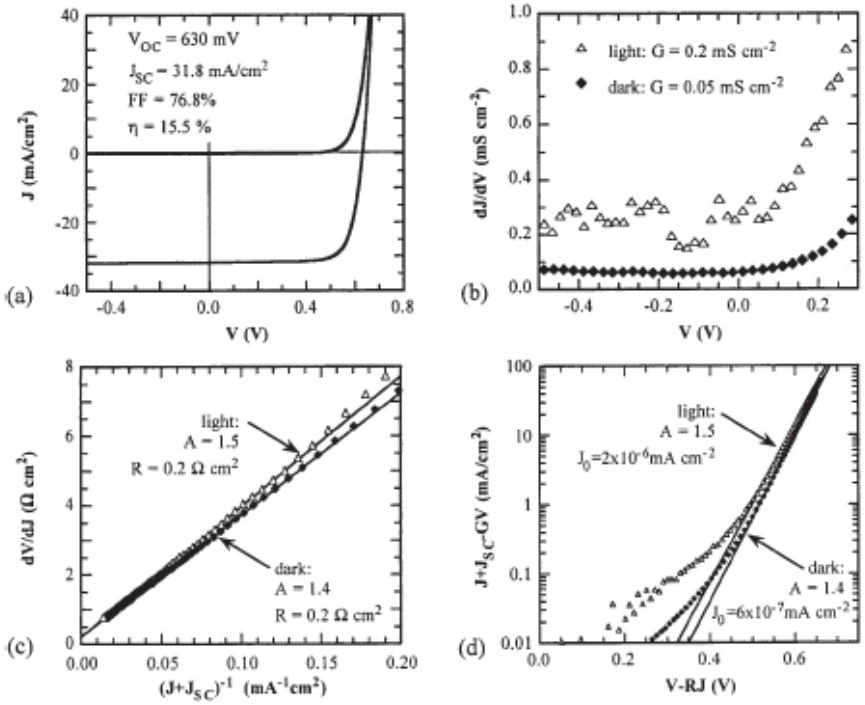


Figure 4.2: Light and dark JV characteristics for a well-behaved CIGS device (a) Standard JV (b) shunt characterization g(V) (c) r(J) with fit used to determine R and n_{id} (d) $\ln(J+J_{sc})$ with fit used to determine n_{id} and J_0. [41]

4.2 Spectral Response and Quantum Efficiency Analysis

It is important to investigate the wavelength dependent current generation in working solar cell devices. The value of J_{sc} from JV measurements represents the photocurrent generation and collection under broad spectrum light. The spectral

response (SR) is similar to the quantum efficiency (QE). The SR represents the ratio of the current generated by the solar cell to the incident optical power [3] and has units of A/W. The QE is the ratio of number of electrons collected per incident photon on the device. Overall, both SR and QE give the spectral dependence of the photo-current collection. The actual measurement process involves the measurement of spectral response from which QE is calculated, hence the QE relates to the SR as:

$$SR = \frac{q\lambda}{hc} QE \tag{4.3}$$

QE ranges from 0 to 1 with a QE of 1 at a particular wavelength indicating that all the incident photons at that wavelength were converted to current; this is the case for an ideal solar cell with no optical (reflection, absorption) or electronic (recombination) losses. QE measurements provide very useful information which about the solar cell and the material from which it was made; the optical losses, bandgap, short circuit current density and sub-bandgap absorption can be determined from QE measurement.

The QE setup consists of an optical system which separates white light into monochromatic light by using a 200 W quartz tungsten halogen EHJ projector lamp, a filter wheel, an Oriel Corner Stone monochrometer, a light chopper and a set of collimating lenses. The cell is mounted on an adjustable stage and electrical contacts are made to the cell by a set of four probes. The probes are connected to an electrical system which consists of IV converter, Stanford Research Labs SR830 DSP lock-in amplifier, a voltmeter, an ammeter and an oscilloscope all interfaced to a computer running the control and data logging software. The optical setup is shown in Figure 4.3 below:

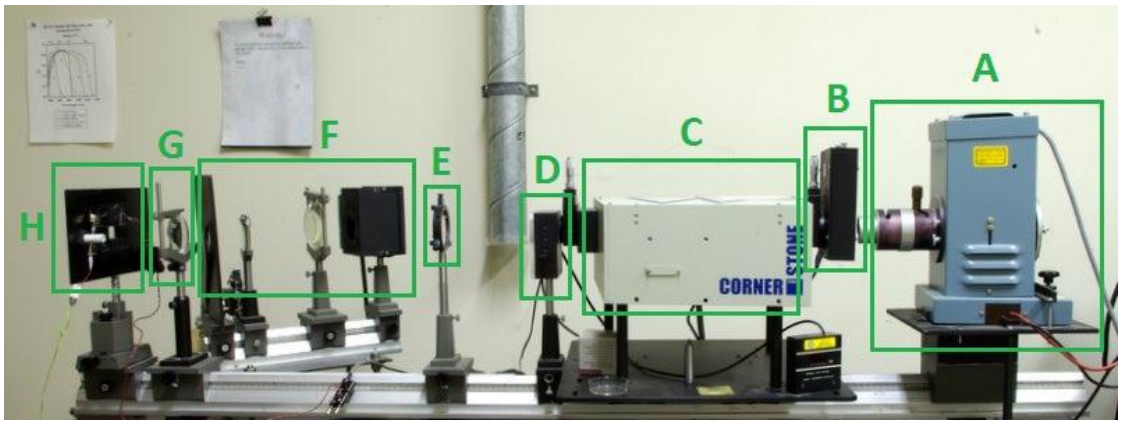


Figure 4.3: QE measurement setup at IEC. (A) Light source, (B) a filter wheel, (C) monochrometer, (D) light chopper, (E) collimating lens, (F) a bias light setup, (G) focusing lens, (H) sample stage.

The light source is incident through a filter wheel which houses long pass filters that removes higher order wavelength interfering modes such that the monochrometer receives light that is free of higher order modes. The monochrometer splits the light into separate wavelengths using gratings which reflects the spectrally dispersed light into a slit producing a Gaussian beam, which is incident on a light chopper, operating at 72 to 78 Hz. The light is then focused on the sample with a collimating and focusing lens. The QE setup also has the capability of applying light and voltage bias which give further insight into losses and response of cells under light induced and voltage bias conditions.

4.3 Capacitance Based Measurements

Capacitance or admittance based measurements are particularly useful for measuring bulk and interface properties in working devices. In thin film devices, these bulk and interface properties could be affected by their working environment and thus films or device layers could exhibit different characteristics when integrated into a

multi-layer thin-film device with junctions, contacts, etc. Surface conditions, interfaces, electric fields and built-in potential may affect electronic properties such as defects in the ACIGS absorber film, spatial uniformity, bulk defect response, density of free carrier, depletion width and light induced metastabilities [42, 43].

4.3.1 Solar cell capacitance/admittance basics

A solar cell is essentially a wide area p-n junction and a lumped circuit model could be assumed with a resistor in parallel with a capacitor [3, 73]. In the small signal approximation differential capacitance could be expressed as:

$$\delta Q = C\delta V \tag{4.4}$$

Where C is the capacitance in Farads (F), Q is the charge in Coulombs (C) and V is the voltage in Volts (V). When a small ac voltage is applied, there are two components of the linear response of the device such that a component is in-phase with the applied voltage and the other out-of phase by 90°.

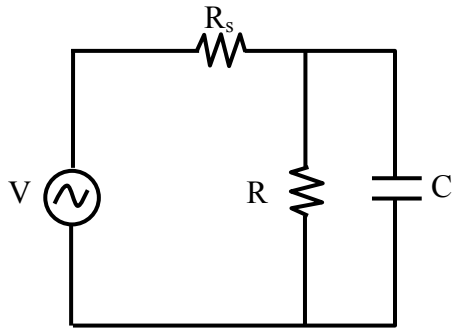


Figure 4.4: Parallel lumped circuit model for device.

The complex admittance could be expressed as:

$$Z = R + jX_c \tag{4.5}$$

Where Z (Ω) is to total impedance, R (Ω) is the resistance, and X_c (=1/jωC) is the capacitive reactance in Ohms. The complex admittance of a device Y(ω) in Siemens is its current response to a small ac signal of angular frequency ω (Hz), where G(ω) is the conductance in Siemens (S) and C(ω) is the capacitance.

$$Y(\omega) = G(\omega) + j\omega C \tag{4.6}$$

The real and imaginary component of the admittance both contains full information of any specific device.

4.3.2 Admittance instrumentation

The setup consists of an Agilent 4284A LCR meter fitted with an external bias module/adapter, a Keithley 2400 source-meter, a digital multimeter (DMM), a Linkam Cryostat (temperature controlled stage) and a computer with control and data logging software as shown in Figure 4.5.

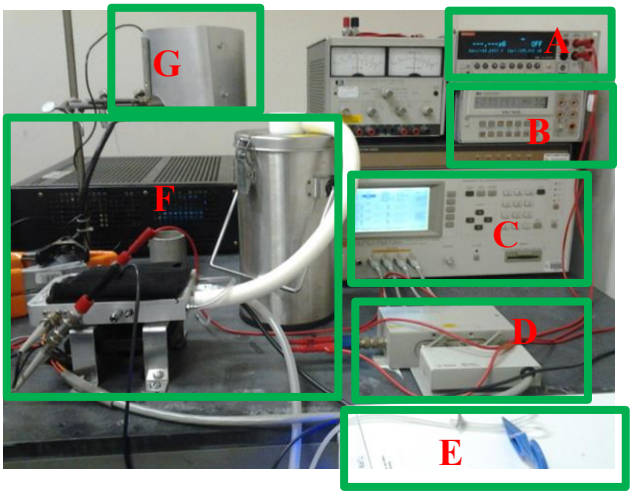


Figure 4.5: Admittance setup showing (A) Keithley 2400, (B) DMM (C) LCR meter, (D) External Bias adapter, (E) Liquid nitrogen pump, (F) Linkam chamber and Nitrogen dewar (G) Light source for JVT measurements

The LCR meter measures the complex admittance (in phase current and current that is 90° out of phase, the Keithley 2400 provides the required external bias to the sample through the external bias adapter, the DMM measures the bias voltage across the sample or DUT, and the Linkam crysostat allows temperature dependent measurements from 200 °C to -180 °C. It contains the DUT which is connected via probes and cables to the electronic meters. The extracted parameters are monitored and recorded by a computer.

4.3.3 Admittance spectroscopy (AS)

Admittance spectroscopy measures capacitance or conductance as a function of applied frequency ω (Hz) and temperature T (K).

The goal is to obtain:

(a) Spatial and energy dependence of densities of states (DOS) or defect density in the absorber layer and

(b) The thermal activation energy of the defects.

(c) Distinguish between bulk and interface defects

As frequency increases, or temperature decreases, the probing or demarcation energy E_e decreases, and deep states can be frozen out, causing an activated 'step' in the admittance profile [44]

$$E_e = kTIn\left(\frac{2\upsilon_0}{\omega}\right) \tag{4.7}$$

A representative plot of capacitance as a function of frequency is shown in figure 4.6.

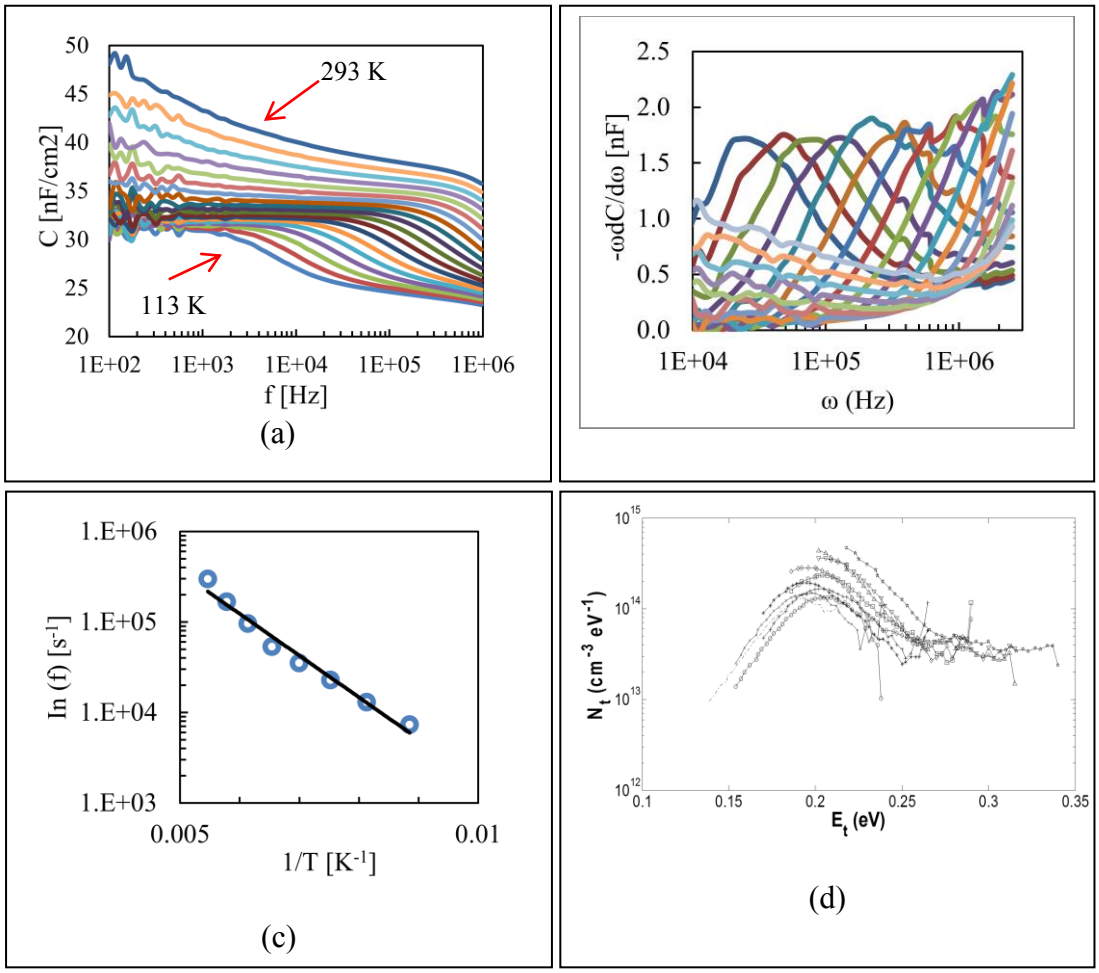


Figure 4.6: (a) Sample AS raw data (C [nF] vs. f [Hz]) for an CIGS device taken in 10K increments from 113 to 293 K (b) Derivative of capacitance indicating characteristic (peak) frequencies at each temperature (c) Arrhenius plot of each peak frequency. A linear fit yields the activation energy, E_a from the slope and the attempt-to-escape frequency, $\nu_{0,}$ from the intercept which are then used to determine distribution of the defect density of states, N_t (d) Sample defect/trap density vs. energetic position for an ACIGS device. Defect peak position is centered around 0.2 eV

In AS, the inability of deep states to respond at a given temperature and frequency, leads to a decrease in capacitance and a step is observed in the C vs. f plot as f is increased or as T is decreased. When deep states can no longer respond, a step in the admittance will be observed, the lower part of the step represents shallow levels, which is just a couple of factors higher than kT (0.025eV), usually 3kT.

The shallow acceptor states represent the doping concentration, while the higher part of the step represents both shallow levels and deep states or defect states usually due to disorder in the crystal structure. In other words, as T increase or f (or ω) decrease, more trap states at deeper energy can begin to respond. The demarcation energy determines the cut-off energy for the trap response at a certain (T, f) point. When the energy of the trap state $E_t = E_e$, the occupation of the state can follow the ac voltage and its charge state will change at the spatial location x_e. This causes the spatial length of charge response, $\langle x \rangle$ to move closer to the interface and C to increase from $\varepsilon\varepsilon_0 A/W$ to $\varepsilon\varepsilon_0 A/\langle x \rangle$. Successively deeper trap states respond as E_e is further increased [3].

4.3.3.1 ACIGS and CIGS absorber

Evidence exists that the addition of Ag reduces the level of disorder and perhaps the defect density in the absorber layer. The admittance technique used here is only capable of probing energy levels well below mid-gap. Capture and emission dynamics determines that for a particular temperature and frequency, only those defects whose energy is less that the demarcation energy can respond to the voltage stimulus and contribute to the measured admittance [46].

While a distinct capacitance step is observed with CIGS films, ACIGS films exhibit a very shallow step or completely flat response to changing frequency and temperature. This may be as a result of reduced shallow state density below mid-gap in ACIGS.

Details of this are discussed in chapters 5 and 6. Some researchers have reported distinct defect features after light soaking the ACIGS devices [23]. The absence of a distinct step AS response for ACIGS cells is very often observed and may be due to the fact that the AS measurement tool and technique misses defects at activation energies beyond its capability [42].

As we increase frequency or lower temperature, the measurements emission energy decreases and tends towards energies closer to the value of the shallow donor level; we thus isolate the deep defects which (in the case of p-type ACIGS) are at energy levels deeper than the shallow acceptor states, making deep states unable to respond. Perhaps a measurement setup with higher sensitivity at low frequencies and moderately high temperature will be capable of probing some deeper states.

According to Walter et al, in order to exclude interface states or spatial inhomogenieties as responsible for the observed frequency dispersion of the capacitance, admittance measurements depending on applied dc bias should be carried out. The activation energy of the distinct step may or may not change and thus could help distinguish between interface and bulk defects. The method involves tracking the activation energy obtained from the Arrhenius plots at different biases for changes: if E_a is constant, the defect is in the bulk, but if E_a changes with bias; the defect is at the interface.

The following steps are employed in the measurement and analysis:

1. Plot C (nF) vs. $\log_{10}$(f) (Hz) at different temperatures, sweeping over a range of frequencies(100Hz to 1MHz) at a particular temperature. Low frequencies are usually neglected because of noise in the data. High

frequencies are not used due to resonance. The effect of resonance in the admittance begins to show as frequency approaches 1MHz [44, 47].

2. Plot $-\omega dC/d\omega$ vs. $\log_{10}(\omega)$ to extract inflection points, or the peak frequencies at the point of defect response step. Conductance information G/ω vs. ω makes the peaks easy to spot but this method could suffer from leakage conductance in the device.
3. Plot an Arrhenius plot of the peak frequencies obtained above, i.e. plot $\ln(\omega)$ $[s^{-1}]$ vs. $1000/T$ $[K^{-1}]$. The Arrhenius relationship could be written as [46],

$$\omega = \upsilon_0 \exp(-E_a/KT) \tag{4.8}$$

where the thermal emission prefactor, ν_0, also called attempt-to-escape frequency or pre-exponential factor is given by

$$\upsilon_0 = N_v(T)\langle v_{th} \rangle \sigma_h \tag{4.9}$$

and $\langle v_{th} \rangle$ is the average thermal velocity, σ_h is the capture cross-section of the gap state involved, N_v is the valance band density of states. The attempt to escape frequency has temperature dependence ($\nu_0 \sim T^2$) arising from the temperature dependence of the thermal velocity, v_{th}, contained in the capture coefficient and the temperature dependence of the effective density of states N_v given by Neumann H., (Sol. Cells 16, 317, 1986) = $10^{19} cm^{-3}$ for CIS. This temperature dependence is usually ignored because it does not affect the results of analysis [44]

4. Find the apparent activation energy (or the trap depth) of the defect E_a (meV) from slope, and, ν_0 the attempt-to-escape from the y-intercept and values are usually in the order of 1E7 s^{-1} to 1E12 s^{-1}.
5. Determine the demarcation energy, E_ω (or emission energy, E_e) using the knowledge of ν_0 and compute and plot the defect distribution, or defect density of states $N_t(E_\omega)$. [44; 45],

$$N_t(E_\omega) = -\frac{2V_{bi}^{3/2}}{W\sqrt{q}(\sqrt{qV_{bi} + (E_g - E_\omega)})}\frac{dC}{d\omega}\frac{\omega}{kT} = c(E_\omega)\frac{dC}{d\omega}\frac{\omega}{kT} \tag{4.10}$$

A known occupation of state defects is established by applying the required bias before measurement; for example, in CIGS, holding a cell under reverse bias (as in before a TPC measurement) will cause defect states in the junction field region to be emptied, whereas a forward bias will allow the capture of majority carriers (holes) into previously empty traps in the depletion region [23]

4.3.4 Mott-Schottky capacitance profiling

Capacitance-voltage profiling also referred to as Mott-Schottky measurements is the most basic measurement made with the capacitance setup. Charge responses to ac signal could emanate from various regions of a device, such as the junction capacitance, deep states and free carriers. A typical procedure will involve measuring capacitance per unit area C/A (F/cm^2) as function of applied dc bias at a high frequency to reduce the possibility of defect responses being included in the measurement. According to a simple electrostatic picture of the one-sided junction

depletion region with a uniform field, the following equation gives the relationship between capacitance and voltage [39, 40]

$$\frac{1}{C^2} = \frac{2}{A^2 \varepsilon_r \varepsilon_0 q N_A}(V_{bi} - V_A) \tag{4.11}$$

From a plot of $1/C^2$ as a function of applied bias as shown in the equation above, the goal is to estimate the depletion width of the device, acceptor doping concentration, N_A (cm^{-3}) in the absorber and the built-in potential. While this is a routine and acceptable method of determining these parameters in crystalline Si devices, the model fails with thin film technologies due to a zoo of deep states present in polycrystalline materials. The consequence of this is an inaccurate estimation of these parameters usually an overestimation occurs. The measured capacitance can be converted to a profile given by [43]:

$$\mathrm{N}_{\mathrm{cv}}(x) = \frac{-2}{A^2 \varepsilon_r \varepsilon_0 q}\left(\frac{d(1/C^2)}{dV}\right)^{-1} \tag{4.12}$$

The profile depth is estimated as

$$\langle x \rangle = \frac{\varepsilon_0 \varepsilon_r A}{C_0} \tag{4.13}$$

Note that CV profiling applies a slowly changing dc bias with a small ac bias superimposed on it, so that the response measured is from the whole device (interface and bulk). Thus standard CV profiling can overestimate the carrier density. Measurements taken at low temperature provide better estimates of the carrier density or free carrier concentration and can be used to distinguish between bulk and interface defects by comparing the profile with that obtained from DLCP. The CV method is

only accurate for materials with little or no deep defect states in the band-gap and is grossly inaccurate for thin films which have a large density of states in the bandgap.

4.3.5 Drive level capacitance profiling (DLCP)

DLCP is immune to interface states and response measured is from the bulk [43], but CV profile measures responses from both deep and interface states. DLCP is unique among ac impedance measurements in that the ac voltage amplitude is varied. In all other measurements the AC voltage remains constant and small, so that small signal approximations apply.

The goal of DLCP is to determine:

a. The energetic and spatial distribution of defects
b. To obtain more accurate estimates of free carrier concentration and defect density
c. To distinguish between metastable changes in the bulk and interface defect densities

DLCP is only sensitive to responses from states within the bulk of the material. Except at certain conditions and energy E_e, at which interface response could be measured in DLCP, it is largely immune to interface states. Hence comparison between CV and DLCP profiles can distinguish interface from bulk response. Since the former is sensitive to all sources of charge within the device or film, changes in interface charge that occurs in dc bias scans in CV affects the accuracy of CV profiles [42, 43].

In CV the relationship between charge and voltage is assumed constant, or more accurately, considered to be slowly varying, so that the equation 4.4 is a good approximation especially since the superimposed ac voltage is usually small, between 25mV and 50mV. At higher ac voltages this relationship fails as we begin to get

responses from states in the bandgap and maybe interface and not just only from the depletion edge. Hence we introduce higher order terms to account for these deep state responses.

$$C = C_0 + C_1 \delta V + C_2 \delta V^2 + \ldots \tag{4.14}$$

A typical measurement and analysis procedure is detailed below:

1. Measure Capacitance C/A [F/cm^2] as function of applied ac bias at fixed dc, then increment the dc bias and repeat.
2. Plot C vs. V_{ac} for each dc bias point and apply a quadratic fit for each plot. The term C_2 is usually ignored because it is negligible and hence its contribution is very small.
3. Determine constants C_0 and C_1 which are the coefficients of the quadratic equation from the fit and are the terms in the equation:

$$N_{DL} = \frac{C_0^{\,3}}{2q\varepsilon A^2 C_1} = p + \int_{E_{f0}}^{E_f + E_e} g(E,x)dE \tag{4.15}$$

4. Plot N_{DL} vs. <x>, where <x>, the profile depth as calculated from the constant C_0 obtained for all the different dc bias points as above.

$$\langle x \rangle = \frac{\varepsilon_0 \varepsilon_r A}{C_0} \tag{4.16}$$

   Most researchers assume values of relative permittivity, ε_r, for CIS to be 11.7 [48] and CIGS and ACIGS to be 13.6.
5. Using the value of υ_0 determined from AS, compute E_e
6. Plot N_{DL} vs. E_e vs. g(E) to get the energetic distribution of states, with g(E) plotted on a secondary axis. A set of N_{DL} values is chosen around a particular value of <x> in the N_{DL} plot e.g. form a set of N_{DL} values by taking all N_{DL}

values on the different N_{DL} curves taken at different frequencies or different temperatures, e.g at <x> = 0.3μm, read off all values on the various curves. The difference between the N_{DL} measured at high and low E_e gives the magnitude of the defect band in cm-3. Continuous defect response can only originate from the bulk. The density of states g(E) is obtained by finding the derivative of the equation for N_{DL} above.

In DLCP, more accurate measurements of carrier density at low temperature is now possible. This is because, low temperature corresponds to low emission energy regardless of frequency. Also for deep states to respond the probing energy must be equal or greater than the energy level of the defect; thus at this condition, deep states have been isolated or "frozen out" and measurement only picks up shallow levels which represent the doping concentration. On the other hand at high T and lower f, which implies higher E_e, the value of N_{DL} measured includes defect and free carrier densities [42].

Capacitance based measurements become much more useful if it is possible to correlate observed defects and carrier density with device performance with the aim of identifying defects which acts as recombination centers and tailoring the processing to reduce the density or impact of those defects.

4.4 Ultraviolet-visible Spectrophotometry (UV-VIS)

The reflectance and transmission measurements were acquired using a Perkin-Elmer Lambda 750 spectrophotometer, fitted with an integrating sphere. The instrument has two light sources, a tungsten lamp (~270nm to ~860nm) and a deuterium lamp (~860nm and above). A combination of filters and a grating monochromator splits the white light into a monochromatic beam. The beam is split

into two, one beam is directed toward the sample and the other is used as a reference. The light beam is then directed to the integrating sphere by a series of lenses. The integrating sphere is shown in Figure 4.7.

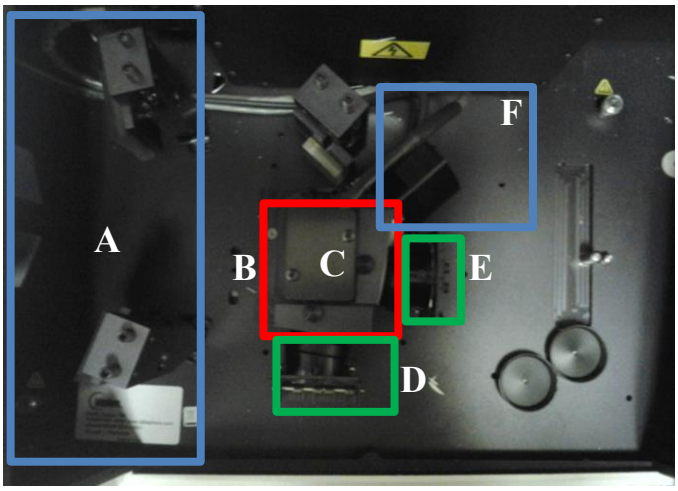


Figure 4.7: (A) Lenses (B) Transmission port (C) Integrating sphere (D) Diffuse reflectance port (E) Reflection port (F) Detector

The arrangement of reflectance disc and samples as well as the nature of the calibration is determined by the specific measurement to be done. For transmission, calibration is done without any sample in the transmission port (B) and that the diffuse Spectralon™ reflection discs are in place at ports E and D. After calibration, the sample is placed (front side up) at the transmission port so that the light can travel through the sample into the integrating sphere C. Calibration for reflection measurements depends on the nature of the sample. If textured, the calibration for transmission described previously will suffice. However if the sample is very specular or smooth, addition configuration settings in the control software is required before

calibration with a highly specular reflector at the reflectance port. This is because; highly specular samples tend to focus the beam on a particular spot on the detector causing the detector to heat up leading to erroneous reflection measurements. This shows up as the normalized transmission, T/(1-R) being greater that 100%.

Figure 4.8 shows a cartoon of the measurement for transmission and reflection.

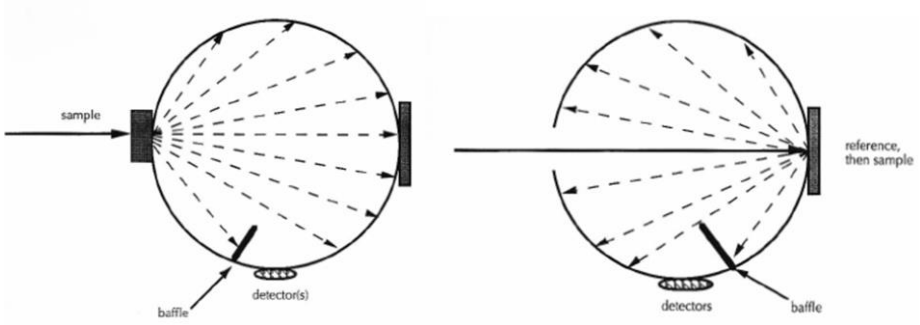


Figure 4.8: (A) Transmission measurement (B) Reflection measurement [49]

Reflection and transmission data obtained is useful for optical loss analysis when combined with QE measurements and for model verification for thin films deposited on glass or Si substrates. The data obtained serves as input to an S-matrix based electromagnetic simulation tool (OPTICAL). Details of the simulations and optical loss analysis are presented in chapters 5 and 6.

4.4.1.1 Small samples

The ability to restrict the beam size is important for accurate measurements of the front reflection of finished devices. The grid and scribed lines could obscure the accuracy of the measurement which will be more accurate and reproducible if the beam is incident only on the TCO/CdS/ACIGS. The beam size traced on a piece of

paper as shown in figure 4.9 below is about 3mm x 15mm which is larger than the open spaces on finished devices as shown in figure 4.10. In this case the calibration has to be done with the mask in place and the reflectance disc behind the mask. Measurements of the masks reflectance were first taken and then the sample was placed behind the mask such that only the beam incident through the mask aperture reached the sample at the reflectance port. The mask reflection is then subtracted from the measurement obtained with the samples to give the correct reflection of the sample.

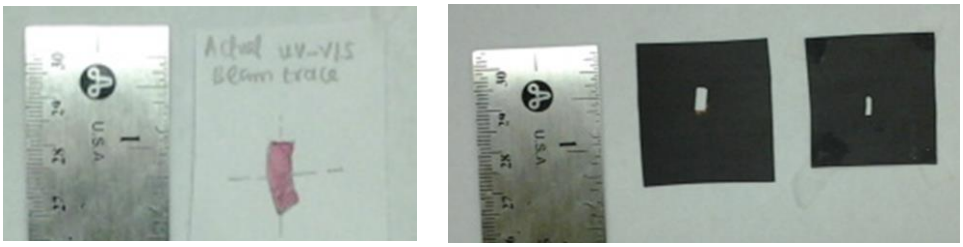


Figure 4.9: (A) Actual UV-VIS beam size traced out on a piece of paper (B) Two masks with different aperture sizes to constrict the light beam.

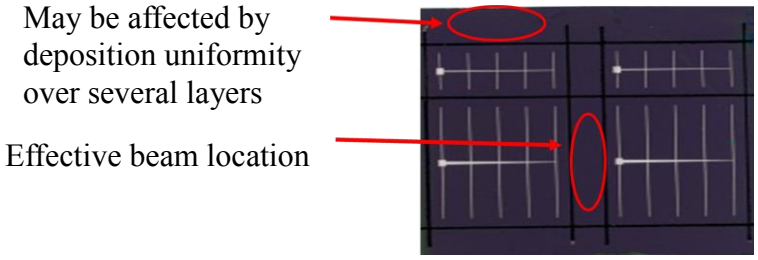


Figure 4.10: Location of beam on finished devices

This procedure was verified by measurements of front reflection on a sample before the top contacts (grids) was deposited to isolated effects of scribing and grid reflections. The result of front reflection measurement for such a sample without grids is shown in figure 4.11.

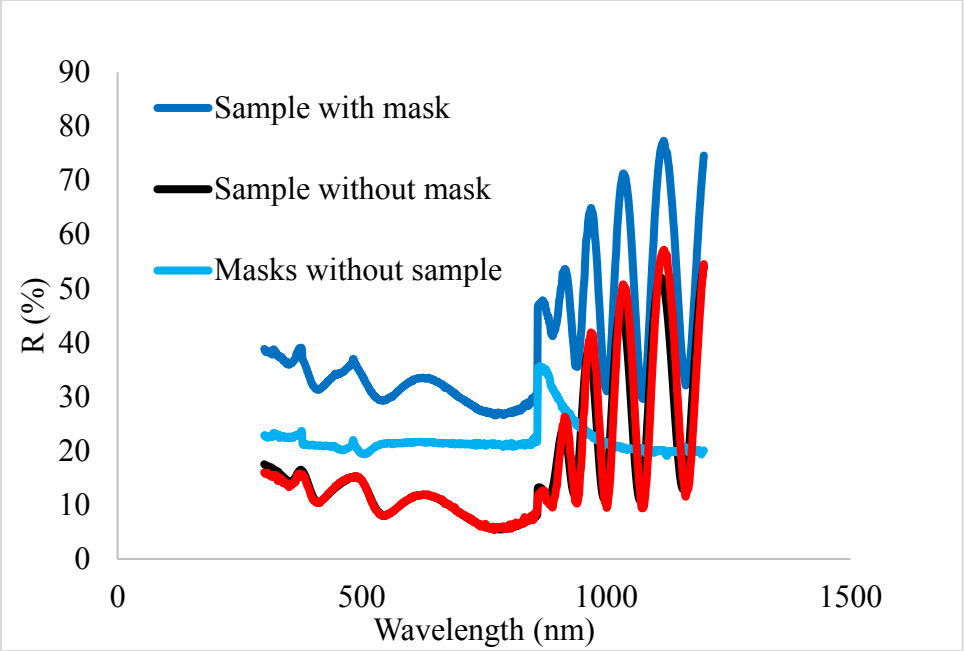


Figure 4.11: Front reflection on a semi-finished device (before grid deposition). The black and red lines are indistinguishable

The black curve represents the front reflection of the sample measured without the mask and the red curve is the front reflection measured with the mask after correction. The correction is done by subtracting the mask reflection only (light blue curve) from the measurement of the front reflection of the device through the mask (dark blue curve). The black and red curve is essentially the same and thus the measurement

made by this procedure is accurate. The technique was then applied to a sample with grids as shown in figure 4.10 and the result is shown below in figure 4.12.

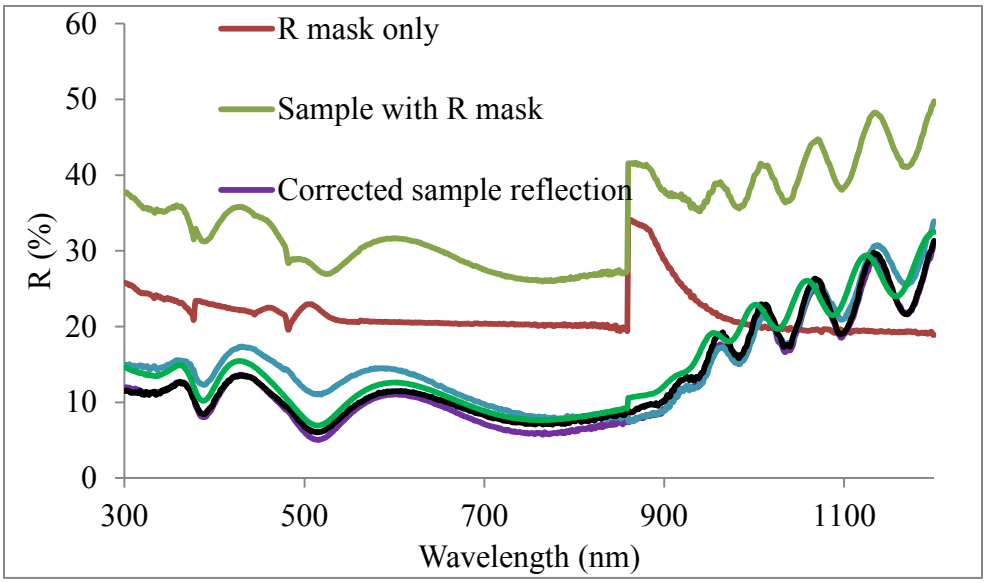


Figure 4.12: Measurement of front reflection from a finished device using a an aperture mask

4.5 Variable Angle Spectroscopic Ellipsometry (VASE)

Optical constants for some layers of the ACIGS device stack were obtained using a J. A. Woollam rotating analyzer variable spectroscopic ellipsometer equipped with an autoretarder. The VASE instrument works by measuring the change in polarization that light waves experience as they are reflected from surfaces and interfaces through planar multilayered materials [50]. These measurements yield a phase difference (Δ) and an amplitude ratio (ψ), which is the complex reflectance ratio of the parallel (r_p) and perpendicular (r_s) wave polarizations, based on the Fresnel equations for reflection and transmission [51]. The complex reflectance ratio (ψ) used

in VASE is measured as a function of both angle and wavelength. The relationship between all these terms is shown in Equation 4.17.

$$\tan(\psi).e^{i\Delta} = \rho = r_p/r_s \quad (4.17)$$

Films deposited on glass were analyzed using variable angle spectroscopic ellipsometry (VASE) measurements. The VASE analysis, involves modeling of material properties using dispersion equations to obtain the optical constants [52, 70]. Complex compositional gradients and roughness could make the process very tedious especially when the samples exhibit inhomogeneous refractive index profiles. The results obtained here are average or bulk or bulk material refractive index. It is very difficult to completely represent the actual working device as surface roughness and can increase the complexity of the electromagnetic computations required, thus, optical constants obtained are compared with transmission and reflection measurements from UV-VIS described above to verify the optical constants.

4.6 Electroluminescence (EL)

Electroluminescence involves the emission of light when a voltage bias is applied to a solar cell. The solar cell essentially behaves as an LED; where injection of minority carriers causes radiative recombination. This recombination mechanism is more likely in direct bandgap materials like ACIGS. The emissions can be detected by a VIS-NIR imaging camera. Being the reciprocal process of a solar cell in operation, cell parameters and phenomena like recombination, shunt resistance, shunt conductance and optical losses also influence the EL measurement. EL could be used as a diagnostic tool on finished devices and a comparison between devices is made in Chapter 6.

4.7 Loss Mechanisms in CIGS Based Solar Cells

It is important to identify and quantify losses in solar cells in order to minimize the overall losses in devices. There is often a tradeoff between these losses; for example making grids wider increases optical shading losses while reducing their series resistance. Losses range from power losses in contact resistance, losses due to lateral current flow in the device structure, losses due to light absorption in buffer and window layers to losses in the back contact. These losses can be experimentally controlled and extracted. Device level measurements offer the best opportunity for improvements in device performance. Such improvements may range from redesigning the solar cell geometry, to modification of the vertical device structure. Thin film in particular has enjoyed the benefit of rapid growth in performance by empirically determined process improvements. A complete understanding of the underlying loss mechanisms is still a major concern for researchers and industry.

While losses could be classified and treated broadly as optical or electronic, some researchers have considered losses in terms of level metrics [53]. The separation of losses into their individual loss mechanisms is critical for quantifying and specifying the losses with respect to a deficit in the specific device parameter as well as the impact of the deficit on overall device performance. Table 4.1 shows a separation of losses in terms of level metrics. Separation of losses enables comparison between devices as well as comparing actual device parameters with theoretical device parameters. Where T_G is the grid transmission and quantifies the fractional power loss due to shadowing by the fingers and grids; τ_r, is the minority carrier life-time; R_f, losses due to front surface reflection; A_{TCO}, absorption losses in the TCO layers, and A_{CdS}, absorption losses in buffer layer; P_{rf} and P_{rb}, fractional resistive losses in fingers and bus bar; P_{cf}, fractional resistive power losses due to contact resistance; P_{tl},

fractional resistive power losses due to lateral current flow; all other symbols are the same as defined previously.

Table 4.1: Separation of losses in working solar cell in terms of level metrics

Level Metric	**Parameter**	**Comment**
First	η	Cell efficiency, the ultimate metric
Second	J_{sc}, V_{oc}, FF	Separates efficiency into its components
Third	n_{id}, J_0, R_s, R_{sh}, V_{bi}, E_a, T_G, R_f, A_{TCO}, A_{CdS}	Constituents of second level metric with physical interpretation
Fourth	τ_r, μ, N_A, ρ, P_{rf}, P_{rb}, P_{cf}, P_{tl}	Directly related to design and processing of individual layers
Fifth	Stoichiometry, E_g, crystal structure	Determines material properties

The higher level metrics determine the lower level metrics with a few exceptions. For example, whereas V_{oc} is not a function of grid transmission (T_G), bandgap determines available current and hence J_{sc}.

While some of the parameters may be difficult to extract accurately, some may require sophisticated measurement techniques, and others may be inferred indirectly. Chapter 6 details the use of some of these level metrics for device comparison.

As mentioned previously losses could also be broadly lumped as electronic or optical as detailed in Table 4.2 below. The list will depend on the device structure considered; here the details of the losses in a typical thin film ACIGS device with substrate configuration are presented.

Table 4.2: Optical and electronic losses in ACIGS devices (substrate configuration)

Optical losses	**Electronic losses**
Grid reflection/shadowing	Incomplete collection
Losses due to front surface reflection (R_f)	Losses due to deep defects, recombination losses
	Series and shunt resistance losses
Absorption losses in the TCO layers (A_{TCO})	Power loss due to grid shadows (P_{sf})
Absorption losses in buffer layer (A_{CdS})	Power loss due to Resistive losses in fingers and bus bar (P_{rf}, P_{rb})
Incomplete generation	Power loss due to contact resistance (P_{cf})
"Unentitled" losses based on E_g	Power loss due to lateral current flow (P_{tl})

Losses associated with the top contact design are analyzed based on work by Martin Green [1].

4.7.1 Optical loss breakdown

The quantum efficiency measurement described in section 4.2 is not only useful for determining the light generated current and optical bandgap of the absorber layer, but also useful for quantification of optical losses also called 'photon accounting'. A combination of QE and measurements of transmission and reflection (T&R) using the UV-VIS described in section 4.4, makes it possible to account for J_{sc} losses, attributing these losses to reflection, absorption and deep penetration losses in finished devices [41, 53]. These losses are detailed in figure 4.13. The large space charge width and high field of a device under reverse bias (-1 V) increases the effective collection length [5] and could be used to overcome incomplete collection in the absorber layer at 0 V bias. At the time of this writing most of the devices made at

the IEC do not suffer from this effect with the QE at 0 V and -1 V being an exact match. A detailed description of the analysis could be found elsewhere [5, 41].

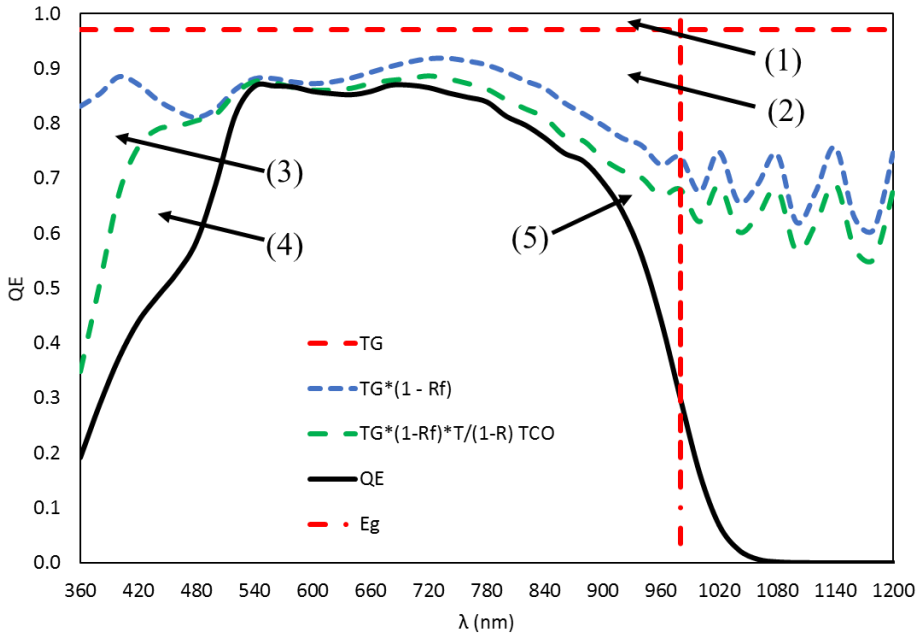


Figure 4.13: Quantum efficiency and optical losses for a typical ACIGS device

Table 4.3: Current loss due to optical and collection losses for a typical ACIGS device, E_g = 1.26 eV and J_{tot} = 36.39 mA/cm^2

Region in Figure 4.11	**Optical loss mechanism**
(1)	Grid shadowing
(2)	Front reflection
(3)	Absorption in ITO
(4)	Absorption in CdS
(5)	Incomplete generation

Table 4.3 lists each of the loss mechanisms encountered (1) – (5), in ACIGS solar cells under this work. Typically an ARC is used to minimize front reflection

The current loss in each case is found by multiplying the respective fractional reflection or absorption loss mechanism, *F(λ)* measured from QE or by UV-VIS with the AM1.5G solar photocurrent [53].

$$J_{loss} = \int_{\lambda_{\min}}^{\lambda_{\max}} F(\lambda) * J_{AM1.5G}(\lambda) d\lambda \tag{4.18}$$

An ideal ACIGS device with a bandgap of 1.26 eV and a QE of 100% will yield a theoretical maximum photocurrent of ~36.39 mA/cm^2. Corrections to the original

4.7.2 Voltage losses

All solar cells regardless of technology have a V_{oc} deficit and it would seem obvious that the path to increased V_{oc} is to solve the defects problem. Accounting for and eliminating the source of this deficit is however not trivial; this is because the fundamental limitations on V_{oc} are not well understood in thin film devices. Overall V_{oc} is limited by the dominant recombination/transport mechanism that dominates the forward current [53]. The roles of defects density and distribution on quasi Fermi level separation, grain boundaries, high J_0, interface states, surface recombination velocity, free carrier concentration, and electrostatic fluctuations could shed some more light on the V_{oc} limitation. Voltage loss due to series resistance, shunt conductance and ideality factor losses could be quantified [54] by taking advantage of the diode analysis procedure described in section 4.1. Open circuit voltage increases with bandgap. By varying the Ga or Ag content, the bandgap could be engineered in ACIGS device. The difference between the bandgap and the ideal open circuit voltage is given by [Rau et al, 1999]

$$E_g - qV_{oc} = n_{id} KTIn\left(\frac{J_{00}}{J_{sc}}\right) \propto n_{id} In(N_t) \tag{4.19}$$

Where J_{00} is a saturation current prefactor which is proportional to the concentration N of recombination centers in the bulk of the ACIGS film and relates to the diode saturation current by

$$J_0 = J_{00} \exp\left[-\frac{\phi_b}{n_{id} KT}\right] \tag{4.20}$$

Where ϕ_b is the barrier height, J_{00} and n_{id} all depend on the recombination mechanism. Typically the barrier is equal to the bandgap in better performing ACIGS devices indicating that the dominant recombination mechanism is Shockley-Read-Hall (SRH) recombination in the quasi-neutral region (QNR) due to deep trap states within the bandgap or at the ACIGS interface [5]. Ideality factor values range from 1 to 2. It is generally accepted that If n_{id} is equal to , then the dominant recombination mechanism is band-to-band recombination and for $1 < n_{id} \leq 2$ SRH recombination dominates.

An empirical relationship shown in equation 4.21 [55] suggests a deficit of 500 mV for CIGS solar cells.

$$\frac{E_g}{q} - V_{oc} = 500mV \tag{4.21}$$

4.7.2.1 Current-voltage-temperature (J-V-T)

It is assumed that the dominant recombination mechanism in ACIGS solar cells is SRH recombination which is largely due to extraneous bandgap states ARISING from compositional or structural defects. With the capability to carry out JV measurements as a function of temperature, one can extract the temperature dependence of the recombination mechanism from a JV curve. Current-voltage sweeps were taken for

several temperatures ranging from 113 K to 313K using the same Linkam cryostat utilized for AS measurement and shown in figure 4.5. The cryostat is LN2 cooled and the chamber is fitted with a temperature sensor and PID controller. The device was illuminated with an ELH lamp calibrated with respect to the J_{sc} of a reference cell from previous STC measurement. Following equation 4.18, one would expect that a plot of V_{oc} (V) vs. T (K) should be linear with an intercept V_{oc} (T = 0 K) approximately equal to E_g. In the case, the dominant recombination path for the device is bulk recombination [3]. A different recombination mechanism can cause the intercept to be less that E_g in which case the diagnosis is that the activation energy extracted is independent of the absorbers bandgap and that the V_{oc} is limited by interface recombination with a barrier = ϕ_b. At low temperature, V_{oc} saturation may be due to a different recombination mechanism or Fermi level pinning or temperature dependent ideality factor effects. If V_{oc} becomes independent of T and intensity, as usually happens, it has to be from 'freeze out' of recombination. V_{oc} is now limited by work functions at the two contacts, not what happens in the junction.

4.7.3 FF losses

The fill factor of a device is affected by recombination in the depletion region mostly by an increase in ideality factor and a decrease in V_{oc} [53]. Fill factor is also affected by voltage dependent collection, $J_L(V)$, series resistance, R_s, and shunt conductance, G. Voltage dependent collection however is negligible in ACIGS device made at the IEC. $J_L(V)$ is due to a change in the collection length under bias and can be determined by observing the JV curve and measuring JV under different light intensities.

In the absence of series resistance or shunt conductance, Martin Green [1] gives an empirical expression for FF with accuracy to about 4 significant digits for

$$FF = \frac{\upsilon_{oc} - In(\upsilon_{oc} + 0.72)}{\upsilon_{oc} + 1} \tag{4.22}$$

Where υ_{oc} is a normalizing voltage given as

$$\upsilon_{oc} = \frac{V_{oc}}{KT/q} \tag{4.23}$$

This simple expression is approximately valid providing that υoc > 10, or Voc > 260 mV. In the presence of series resistance, the FF is given as [53]

$$FF_s = FF(1 - R_s / R_{ch}) \tag{4.24}$$

Where the characteristic resistance, $R_{ch} = V_{oc}/J_{sc}$.

When series resistance and shunt conductance are not negligible, then equation 4.22 becomes [53]

$$FF_{s+sh} = FF_s \left[1 - \frac{(\upsilon_{oc} + 0.72) FF_s}{\upsilon_{oc} / (R_{ch} G)} \right] \tag{4.25}$$

Chapter 5

ELECTRONIC AND OPTICAL SIMULATION

Numerical modeling is a very useful tool in solar cell design and fabrication as it provides insight into the details of device operation and physics. The viability of proposed physical explanations due to physical changes made to a solar cell device could be correlated with the cell performance. However, polycrystalline CIGS thin-film solar cell simulation can be quite a difficult task to undertake due to the complex device physics involved and lack of accurate known values for many of the input parameters. Various aspects of the device have to be considered, as a tradeoff is usually made when optimizing the optical and electrical performance of devices. Solar cells are inherently complex devices comprising of several layers, surfaces and interfaces which could be very difficult to model accurately. Polycrystalline thin-film solar cells are even less well described or characterized. However, device simulation tools have been developed and most of the issues with electronic simulations have come a long way from 1D to 3D simulations. Burgelmann et al [56] presents a detailed comparison of the various simulation tools available to the PV community, highlighting their successes and limitations. Some of the limitations discussed have been resolved over the past decade and these simulation tools are considerably more mature in their applications and results. At the time of this writing, multilayer optical simulation which focuses on improving optical path length especially in thin-film CIGS superstrate configurations has started receiving significant attention [52]. This chapter focuses on modeling optoelectronic properties of finished devices using a

numerical approach and employs optical multilayer simulations for thickness determination of thin films that form part of the device structure specifically ITO and i-ZnO. Variations in the optical properties of i-ZnO layer are studied based on thickness and sheet resistance experiments described in chapter 2.

5.1 Electronic Simulations

Simulations of electro-optical measurements were routinely carried out on finished devices. Current-voltage (JV), capacitance and (QE) was performed and applied to model record CIGS-based devices and to compare devices fabricated in this thesis.

5.1.1 Software

Simulations of complete solar cell devices was carried out based on a numerical simulation approach using the Solar Cell Capacitance Simulator (SCAPS) developed and maintained at the University of Gent [57]. At the time of the writing the most recent version of this software is SCAPS 3.3.00 released in August 2014. This software is specifically designed for modeling thin-film polycrystalline CdS/CdTe and CdS/CIGS based devices by solving the Poisson's and continuity equations for electrons and holes [40]. The program is able to simulate the dc and ac electrical characteristics of thin film heterojunction solar cells. Several layers can be included to 7 layers and 6 interfaces and the layer properties are alterable. Interface and bulk defects, grading and fundamental material properties like mobility, effective density of states and thermal velocity are well accounted for. Measurements including JV, CV, C(f) and QE can be simulated for light and dark conditions and as a function of temperature.

5.1.2 Material properties and input parameters

The Baseline parameters representing the CIGS absorber layer are chosen based on device and material characterization at the IEC and significant work published in the literature [23, 58, 59, 60, 61, 57, 62]. First the defect parameters are chosen for each layer in the standard CIGS solar cell structure, to yield device parameters similar to the record efficiency cell [63, 71, 72] shown in table 5.1.

Table 5.1: Confirmed record ZSW CIGS cell parameters measured at FhG-ISE and simulated device in SCAPS

	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)	Area (cm^2)
ZSW	0.730	35.77	77.7	20.3±0.6	0.5005
Simulated	0.723	35.42	79.7	20.42	-

The key device and layer parameters necessary for the simulation and used for record devices are displayed in table 5.1, where, R_f is the front surface reflection; d, is the absorber layer thickness; Φ_{be} and Φ_{bh} are the electron and hole barrier height in the front and the back of the device respectively; E_g is the bandgap; μ_e and μ_h are the electron and hole mobility; N_C and N_V are the conduction and valence band effective density of states; S_e and S_h is the electron and hole surface recombination velocity respectively; χ is the electron affinity; N_A and N_D is the shallow doping acceptor and donor density; N_t is the recombination defect density; E_t recombination defect peak energy level; and ϵ and ϵ_0 is the material and vacuum permittivity. The parameters used here have been carefully selected to represent device behavior as accurately as possible, thus establishing a realistic parameter set for subsequent simulation.

Table 5.2" Simulation input parameters for record CIGS devices

Layer Properties	**CIGS**	**CdS**	**i-ZnO**	**ITO**
d (μm)	2.7	0.05	0.05	0.15
E_g (eV)	1.2	2.4	3.2	3.4
μ_e (cm^2/Vs)	50	50	50	50
μ_h (cm^2/Vs)	20	20	20	20
N_C (cm^{-3})	2.2×10^{18}	2.2×10^{18}	2.2×10^{18}	1×10^{20}
N_V (cm^{-3})	1×10^{19}	1.8×10^{19}	1.8×10^{19}	1×10^{20}
ϵ/ϵ_0	13.6	10	9	9
N_A (cm^{-3})	1×10^{16}	1	1	1
N_D (cm^{-3})	1	1×10^{17}	1.2×10^{16}	5×10^{19}
χ (eV)	4.50	4.450	4.445	4.5
Defect States				
Type *Profile* *Distribution* *N_t (cm^{-3})* *E_t (eV)*	Acceptor Uniform Single 1×10^{14} E_v+0.3	Donor Uniform Single 1×10^{17} E_v+1.2	Donor Uniform Single 5×10^{17} E_v+1.7	-
σ_e (cm^2)	1×10^{-13}	1×10^{-17}	1×10^{-12}	-
σ_h (cm^2)	1×10^{-15}	1×10^{-12}	1×10^{-15}	-
General device properties				
S_e (cm/s)	10^7	10^7	10^7	-
S_h (cm/s)	10^7	10^7	10^7	-
R_s (Ωcm^2)	0.23			
r_{sh} (Ωcm^2)	1500			
R_f	5%			
Grid reflection	4%			
Φ_{be}, Φ_{bh}	Flat bands			
Absorption model	Gloeckler baseline	CdS-base	ZnO Adachi and Malmstroem	-

The simulation results of JV and QE for the current record CIGS record is presented in figure 5.1. These results were obtained using the parameters detailed in table 5.2. Devices with efficiency greater than 20% have been fabricated at ZSW for a bandgap range of 1.16 to 1.2 eV [9].

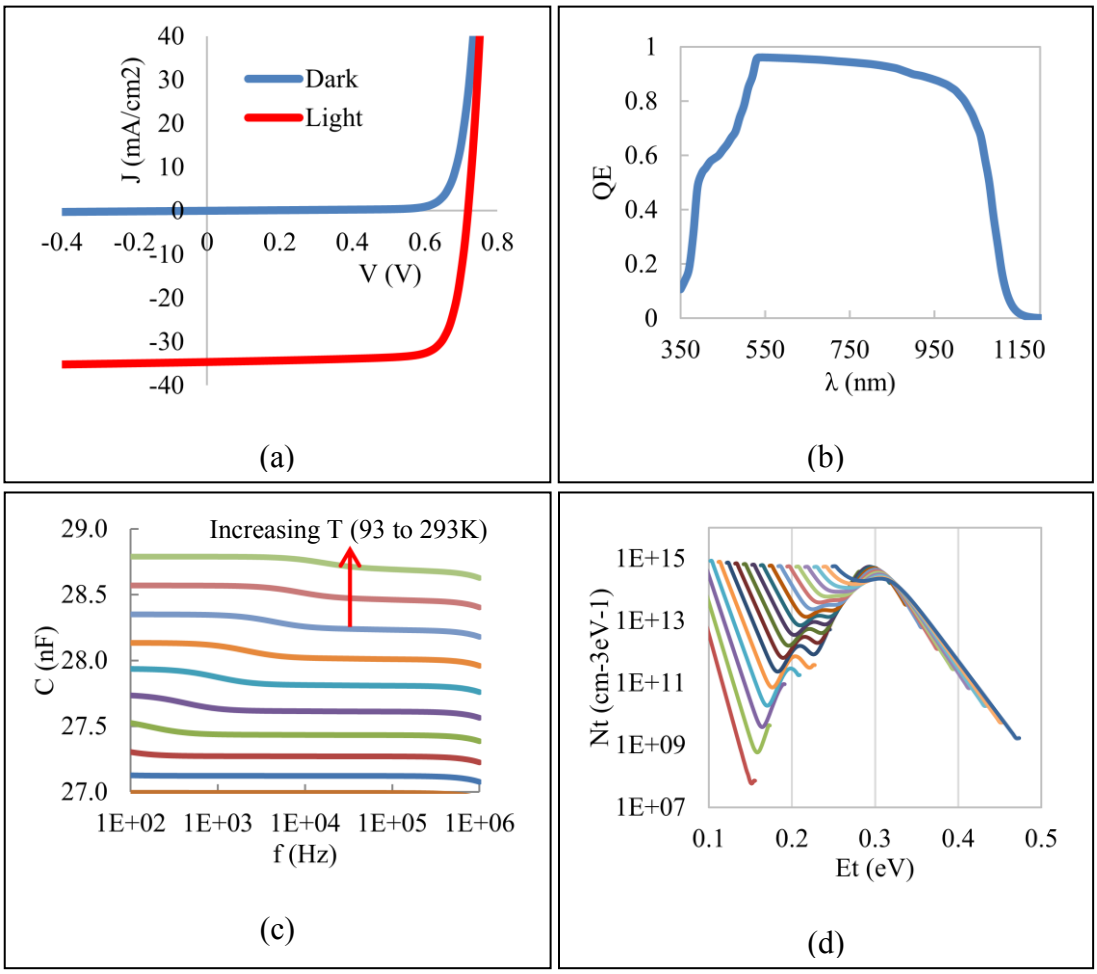


Figure 5.1: Simulation output for record cell devices (a) JV (b) QE (c) Capacitance as a function of frequency show a shallow step in capacitance response (d) Defect density and position as a function energy

The current loss due to CdS absorption is minimal in the blue region and the QE is slightly lowered toward long wavelength. The total available current for a bandgap of 1.2 eV using the AM1.5G spectrum is ~39.5 mA/cm^2.

5.1.3 Simulation assumptions

While a number of assumptions are used in the analysis of thin-film CIGS devices as one-sided p-n junctions, this section focuses on mentioning a few assumptions made in the simulation process. What follows is a list of a few assumptions: contacts are assumed ohmic, reflection at back contact insignificantly affects current generation, back and front contact surface recombination velocities, S (cm/s) are equal to the thermal velocity of carriers and minority carrier concentrations are far less than majority carrier concentration in the respective layers, i.e. low level injection for all bias conditions.

5.1.4 ITO/i-ZnO/CdS/CIGS structure

Device performance greater than 20% efficiency suggests a very good quality absorber with benign grain boundaries and reduced mid-gap state density. To achieve this, a Gaussian distributed acceptor type defect at 0.3eV above E_v is set in the simulation input parameters. The capacitance as a function of frequency and the computed defect density measured by admittance is shown in figure 5.1.

The best CIGS device made at the IEC at the time of this writing is a 17.5% efficient device as shown in table 5.3; the typical CIGS baseline process yields devices in the 15.5 to 16.5% range. Device characterization suggests that these devices are dominated by SRH recombination in the absorber. The IEC baseline CIGS cells were simulated to reflect the lower performance compared to record devices. Reduced performance was achieved by leaving most of the basic semiconductor parameters in table 5.2 the same, increasing the defect density, and adding detrimental effects like interface defects and or moving the defect energy level toward mid-gap.

Table 5.3: IEC CIGS record device and simulated device results

	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)	Area (cm^2)
IEC CIGS	0.698	32.50	76.90	17.50	1
Simulated	0.682	33.03	76.94	17.35	-

The changed parameters from table 5.2, used for the simulation are presented in table 5.4 below:

Table 5.4: Simulation input parameters for record CIGS devices

Layer Properties	**CIGS**	**CdS**	**i-ZnO**	**ITO**
N_A (cm^{-3})	5.5×10^{15}	1	1	1
N_D (cm^{-3})	1	1×10^{17}	1.2×10^{16}	5×10^{19}
Defect States	**CIGS**			
Type	Acceptor	Acceptor	Donor	
Profile	Uniform	Uniform	Uniform	
Distribution	Single	Single	Single	
N_t (cm^{-3})	1.4×10^{14}	8.0×10^{13}	5.0×10^{13}	
E_t (eV)	E_v+0.3	E_v+0.6	E_v+0.8	
σ_e (cm^2)	1×10^{-13}			
σ_h (cm^2)	1×10^{-15}			
General device properties				
R_s (Ωcm^2)	0.3			
r_{sh} (Ωcm^2)	1000			
R_f	8%			
Grid reflection	4%			

Parameters like recombination defects density, type and level in the CdS and window layers were unchanged. The simulated JV, QE and admittance response is shown in figure 5.2 below.

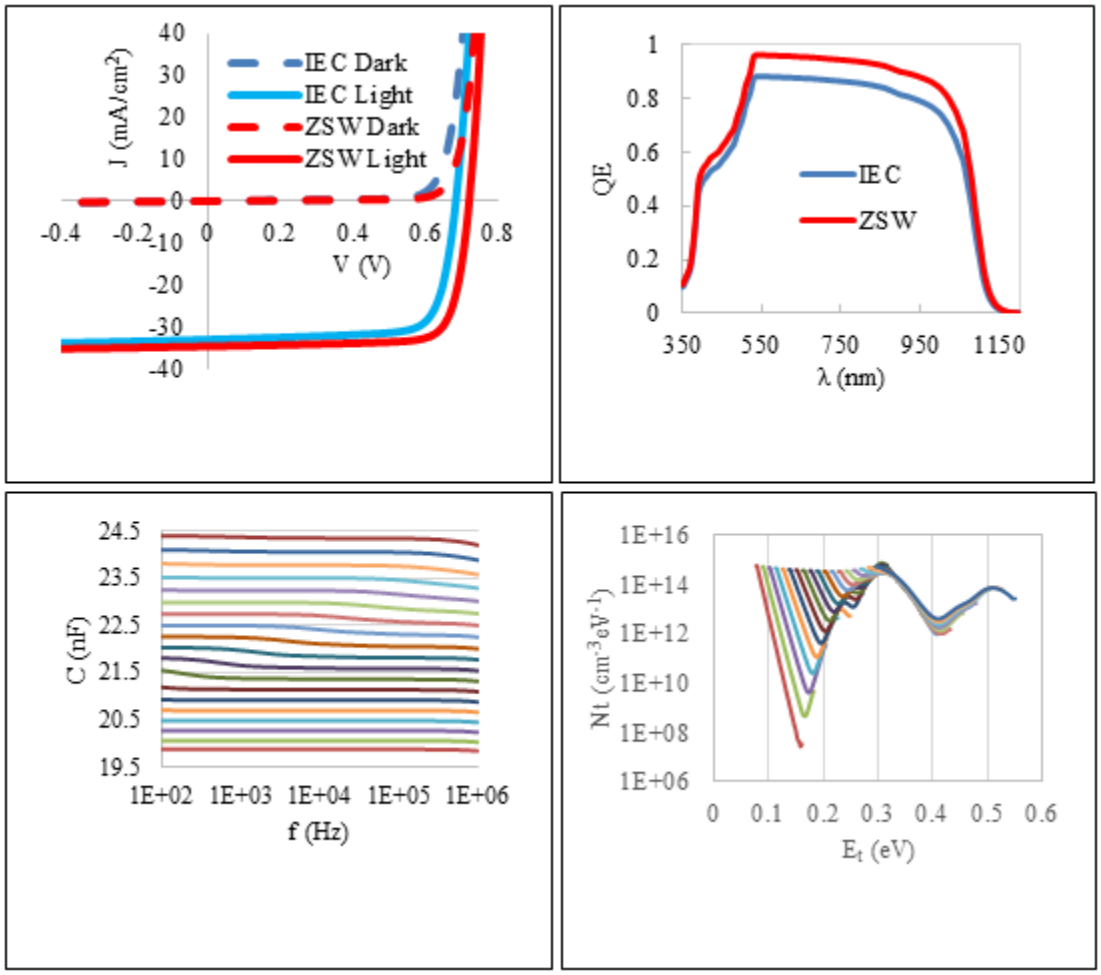


Figure 5.2: Simulation output for IEC CIGS device (a) JV (b) QE (c) Capacitance as a function of frequency (100Hz – 1MHz) and temperature range 113 K to 293 K (d) Defect density and position as a function energy

CIGS devices fabricated and characterized by DLCP indicate free carrier density of 1E15 to 5.5E15 cm^{-3} compared to record devices (1E16 cm^{-3}). Using the established simulation parameters for record cells, changing only the carrier concentration to 5.5E15 cm^{-3} decreased the V_{oc} by 15 mV. The admittance response is typical of fabricated CIGS solar cells measured with an LCR meter as discussed in chapter 4. Detecting deep state response will require measurement equipment with higher sensitivity at low frequencies as practical measurements are limited by noise at low frequencies. In the AS response shown in figure 5.3 below, the simulation frequency range has been expanded, from 1Hz to 100GHz.

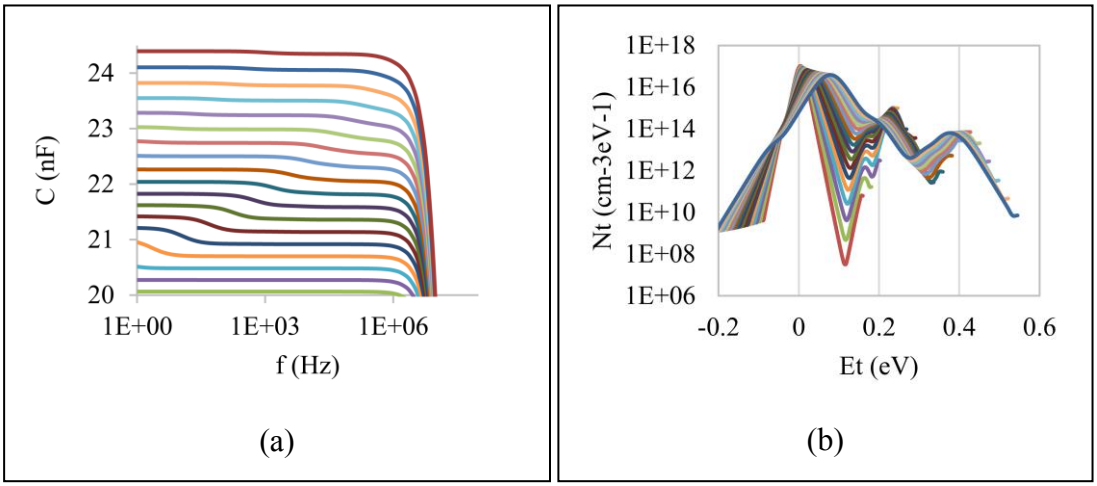


Figure 5.3: Admittance spectroscopy for simulated IEC CIGS sample, T is 93 to 293 K at 0 V bias, frequency range in simulation is 1Hz to 1000GHz ,which is mostly not practical at the time of this writing (a) C(f) (b) Trap density and distribution as a function of energy; peak density is indicated by maxima in the profile.

As the frequency is decreased and temperature increased or vice versa, deep states or traps can be "frozen-out" or can begin to respond and hence a step in the capacitance is observed. In practice measurements at very low and high frequency are obscured by noise and resonance in and from measurement equipment and connecting wires. Measurements on actual fabricated devices are presented in chapter 6.

5.1.5 ITO/ZnO/CdS/ACIGS structure

The baseline simulation model established for the case of CIGS above was extended to simulate ACIGS devices, with slight modifications to the CIGS model in order to account for the experimentally observed effects of Ag alloying. The major differences between both material systems based on Ag alloying efforts at the IEC and as published in literature are

a) Free carrier concentration (N_A) of ACIGS is relatively lower compared to CIGS as measured by DLCP [23]
b) Deep defect density decreases as measured by transient photo capacitance (TPC). Details of TPC are found elsewhere [58]. The characteristic slope (Urbach edge) has been measured to be between 10 and 20 meV which is much steeper than corresponding CIGS samples. This suggests that addition of Ag may be reducing the degree of disorder in the baseline CIGS alloy.
c) Processing devices with wider bandgap via Ag is therefore possible without detrimental effects of increasing bandgap by Ga addition, which manifest by devices showing a voltage dependent light generated current and worsened transport and lifetime properties [64, 65]

The significance of Ag addition to the CIGS baseline samples simulated in section 5.1.4 has manifested consistently as an increase in device performance at the IEC for CIGS and ACIGS of the same bandgap. The champion device fabricated at the IEC as at the time of this writing is an 18.3% device as detailed in table 5.5

Table 5.5: IEC ACIGS record device and simulated device results

	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)	Area (cm^2)
IEC ACIGS	0.752	31.20	77.90	18.30	1
Simulated	0.749	31.73	77.77	18.49	-

From a) and b) above, the simulation for ACIGS was performed using relatively lower carrier density (4E14 cm^{-3}) and lower density of deep defects, compared to CIGS. The bandgap was also increased to 1.3 eV. Details of simulation parameters are presented in table 5.6.

Table 5.6: Simulation input parameters for record ACIGS devices

Layer Properties	**ACIGS**	**CdS**	**i-ZnO**	**ITO**
E_g *(eV)*	1.3	2.4	3.2	3.4
N_A *(cm^{-3})*	4×10^{14}	1	1	1
N_D *(cm^{-3})*	1	1×10^{17}	1.2×10^{16}	5×10^{19}
Defect States	**ACIGS**			
Type	Acceptor	Acceptor	Donor	
Profile	Uniform	Uniform	Uniform	
Distribution	Single	Single	Single	
N_t *(cm^{-3})*	6×10^{12}	5×10^{13}	1×10^{13}	
E_t *(eV)*	E_v+0.3	E_v+0.6	E_v+0.85	
σ_e *(cm^2)*	1×10^{-13}			
σ_h *(cm^2)*	1×10^{-15}			
General device properties				
R_s *(Ωcm^2)*	0.3			
r_{sh} *(Ωcm^2)*	1000			
R_f	8%			
Grid reflection	4%			

Figure 5.4 shows the admittance spectroscopy for the resulting ACIGS device. A lower capacitance and flat admittance response, i.e., no distinct step in capacitance as a function of frequency is characteristic of fabricated devices.

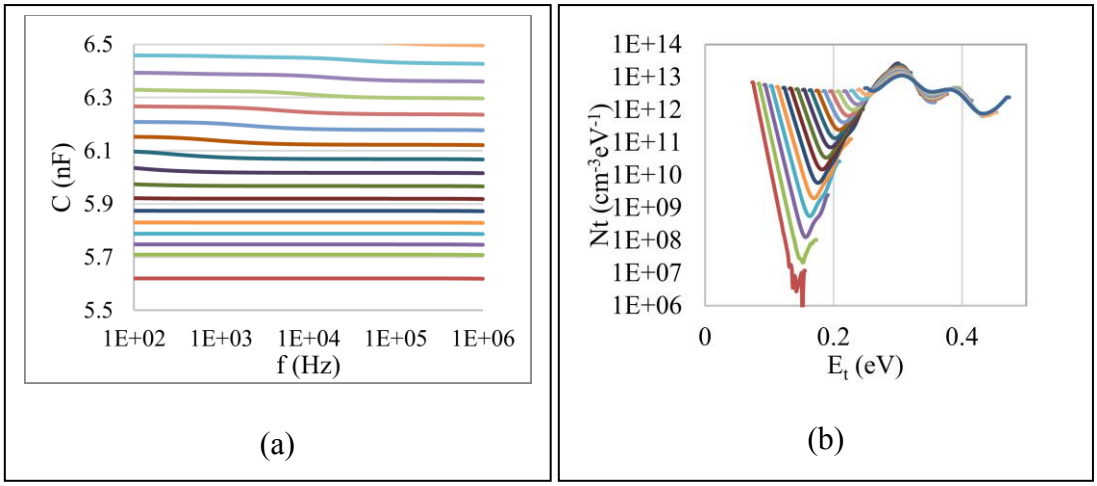


Figure 5.4: AS response for ACIGS device (a) C(f) with very shallow response from defect states typical of fabricated ACIGS devices (b) Trap density and distribution showing lower trap peak energies and distribution

Using the same simulation parameters except changing the absorber free carrier density from 5.5E15 to 4E14 cm^{-3} led to a decrease in V_{oc} of 40 mV. Increasing the bandgap by 0.1 eV from 1.2 to 1.3 eV, yielded a 100 mV increase in V_{oc}. Practically, although the 1:1 gain in V_{oc} with bandgap increase is experimentally observed, the simulated devices do not suffer depreciation in transport properties as observed in fabricated CIGS devices, perhaps due to the addition of Ag. ACIGS devices fabricated at the IEC are optimized around a 50% Ga/(In+Ga) ratio. It is however important to note that the V_{oc} deficit is still quite large, probably due to deep states present in these devices. The V_{oc} deficit will be covered in chapter 6.

The simulation setup for ACIGS devices was then used to study the effect of changing the thickness and sheet resistance of the i-ZnO layer in the section which follows.

5.2 Effects of i-ZnO Thickness and Sheet Resistance on Device Capacitance and Depletion Width

Using simulation parameters for ACIGS, the properties of the i-ZnO window layer were changed and the effect on device parameters was studied. Details of the deposition method are found in chapter 2 while details of the design of experiment and results are found in chapter 6. This section will focus on the simulation of these effects and the output will be presented and discussed briefly.

5.2.1 Effect of i-ZnO thickness

The simulation parameters for ACIGS following the above discussion in section 5.1 were used to investigate the effect of the i-ZnO thickness on the capacitance and depletion width, hence the field distribution in the device. The capacitance sweeps are taken at 100 KHz and in the dark and the value of the capacitance at 0 V bias (C_0) is recorded from which the depletion width, w, is calculated using

$$C_0 = \frac{\varepsilon\varepsilon_r A}{w} \tag{5.1}$$

Table 5.7 summarizes the input parameters and results of simulation.

Table 5.7: Thickness of i-ZnO and its impact on device parameters

i-ZnO thickness (nm)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)	C_0 (nF)	w (μm)
0	0.749	32.08	77.78	18.70	6.796	1.77
10	0.749	32.00	77.78	18.66	6.695	1.80
30	0.749	31.85	77.77	18.57	6.696	1.80
50	0.749	31.73	77.77	18.49	6.696	1.80
100	0.749	31.46	77.76	18.33	6.696	1.80

An efficiency variation of ~0.4% is observed which is within the margin of error hence the simulation indicates that for an absorber layer with N_A of 4E14 cm^{-3}, changing the thickness of the i-ZnO within the range of 0 to 100 nm for may not have a significant effect on device performance. The JV characteristics and capacitance as a function of applied bias are presented in figure 5.5.

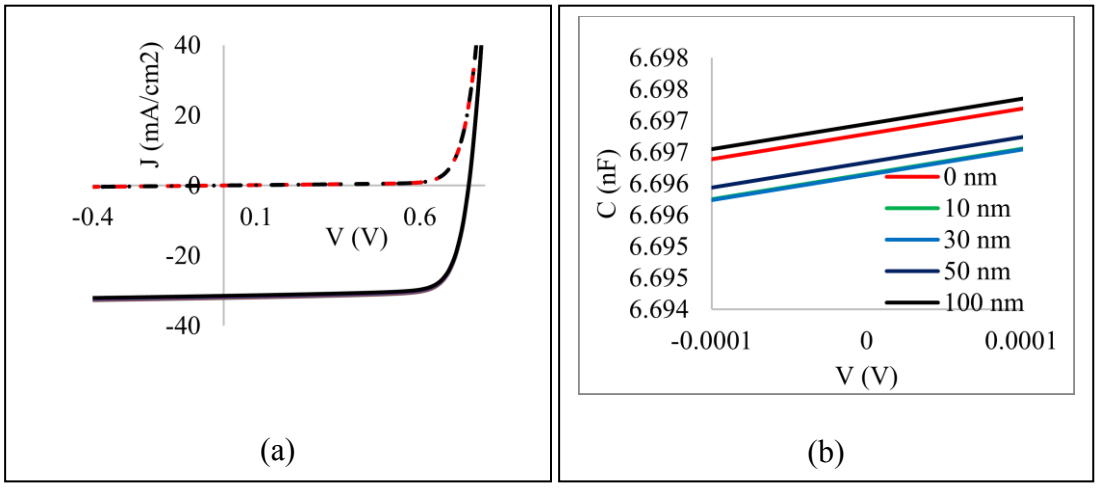


Figure 5.5: (a) JV characteristics for devices with i-ZnO thicknesses, 0, 10, 30, 50 and 100 nm (b) CV for devices with i-ZnO thicknesses, 0, 10, 30, 50 and 100 nm (Observe the scale on the axes, the graph is zoomed-in around 0 V).

5.2.2 Effect of ZnO resistivity

The sheet resistance of the i-ZnO layer was changed by depositing the layer from an Aluminum doped Zinc oxide (AZO) target as described in chapter 2. The thickness of the AZO was kept constant at 50 nm, while the percentage oxygen was varied. The resistivity of the films was calculated from the knowledge of the sheet resistance and the thickness and the carrier concentration was inferred using the assumed mobility

values [61] used in the table 5.2. The computation is shown in table 5.8. The calculated values of N_A are then used as input for the simulation, where the doping concentration of the i-ZnO layer is varied and the device parameters calculated.

Table 5.8: Calculated carrier concentration from sheet resistance, assuming a constant mobility of 50 cm^2/V-s. The 4 values of R_{sh} are selected to match those obtained experimentally.

R_{sh} (Ω/□)	**~2 M (Control)**	**138 K**	**35 K**	**800**
ρ (Ω-cm)	1.00E+01	6.90E-01	1.75E-01	4.00E-03
σ (S/cm)	1.00E-01	1.45E+00	5.71E+00	2.50E+02
N_A (cm^{-3})	1.25E+16	1.81E+17	7.14E+17	3.13E+19

The JV parameters and capacitance data are shown in table 5.9 and figure 5.6.

Table 5.9: Sheet resistance of AZO and its impact on device parameters for N_A = 4E14 cm^{-3}.

i-ZnO sheet resistance (Ω/□)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)	C_0 (nF)	w (μm)
800	0.761	31.73	77.77	18.49	6.696	1.80
35 K	0.749	31.73	77.77	18.49	6.696	1.80
138 K	0.749	31.72	77.76	18.49	6.695	1.80
~2 M	0.749	31.73	77.76	18.49	6.695	1.80

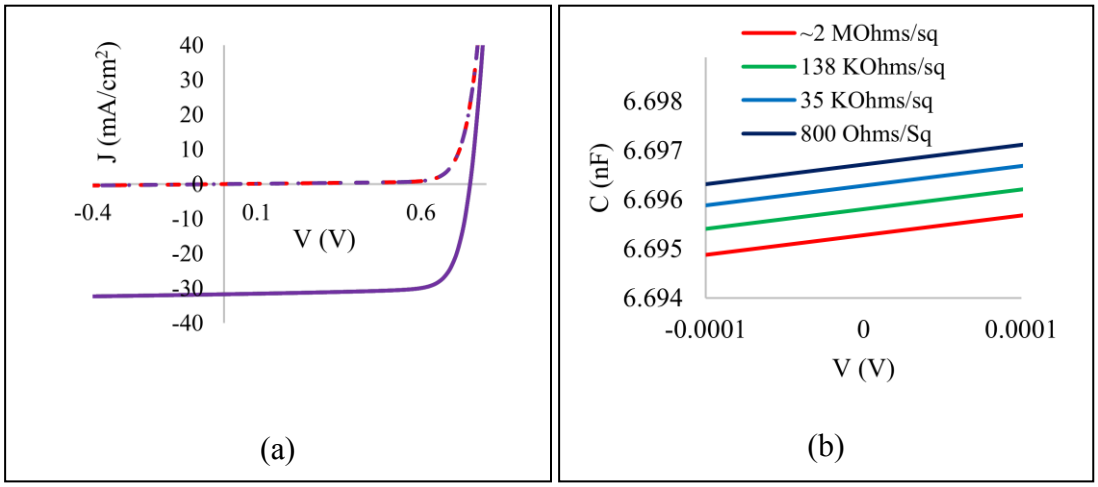


Figure 5.6: (a) JV characteristics for devices with AZO sheet resistances, 2 M, 138 K, 35 K and 800 Ω/□ (b) CV for devices with AZO sheet resistances, 2 M, 138 K, 35 K and 800 Ω/□ for N_A = 4E14 cm^{-3}. (Observe the scale on the axes, the graph is zoomed-in around 0 V).

The same simulation procedure was repeated with higher absorber free carrier density (as in CIGS devices, 1E16 cm^{-3}) and the results are presented in table 5.10 and figure 5.6 below.

Table 5.10: Sheet resistance of AZO and its impact on device with higher carrier density (N_A = 1E16 cm^{-3})

AZO sheet resistance (Ω/□)	C_0 (nF)	w (µm)
800	28.94	0.42
35 K	28.34	0.42
138 K	27.99	0.43
~2 M	27.57	0.44

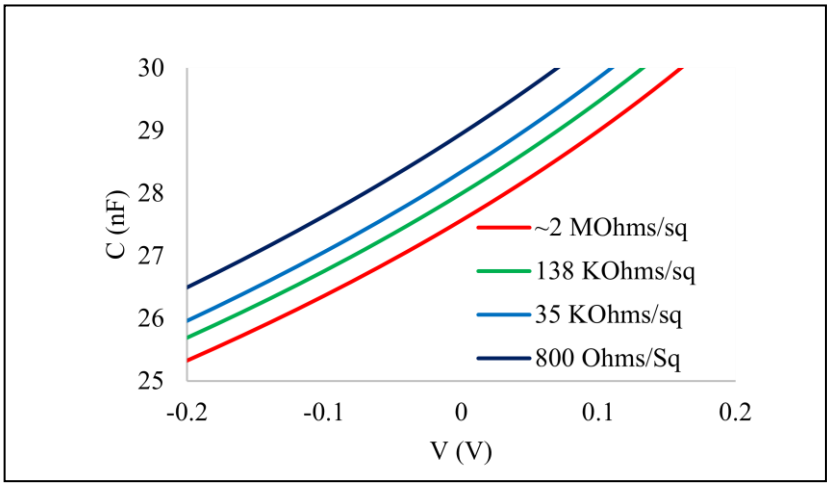


Figure 5.7: CV for a device with N_A of 1E16 cm^{-3}, and AZO sheet resistances, 2 M, 138 K, 35 K and 800Ω/□

The overall device capacitance is increased with increase in absorber carrier density as shown in figure 5.7. A relatively larger change in capacitance with AZO sheet resistance is also observed. The device depletion width is smaller compared to the ACIGS devices as expected for a fixed CdS doping concentration. The simulation predicts a higher V_{oc} and FF for this device and a slightly lower current, but the potential increase in overall efficiency of about 1%.

5.3 Optical Simulation

Optical simulations of individual layers in the solar cell stack were done using Optical Software [66]. The software is an electromagnetic simulation tool which tackles the multilayer problem, using the s-matrix algorithm described elsewhere [67]. The program is capable of accepting input from other measurement techniques like VASE and T&R described in chapter 4. This feature allows direct comparison of

simulations with experiment. The program also used light energy flux as against intensity for absorption measurements enhancing accuracy and speed. Data points from computations are written to an output file which can be saved and manipulated as required.

Optical constants for, ITO and i-ZnO were obtained by VASE and used as input to simulate the reflection, transmission and absorption (RTA) of the films. Simulated RTA were compared with RTA measured using the UV-VIS. This technique was used to estimate the thickness of the layers. The thickness parameter in the simulation interface was adjusted to get a good fit to the measured RTA profiles. Figure 5.8 below shows simulated and experimental RTA data for ITO/i-ZnO/SLG stack.

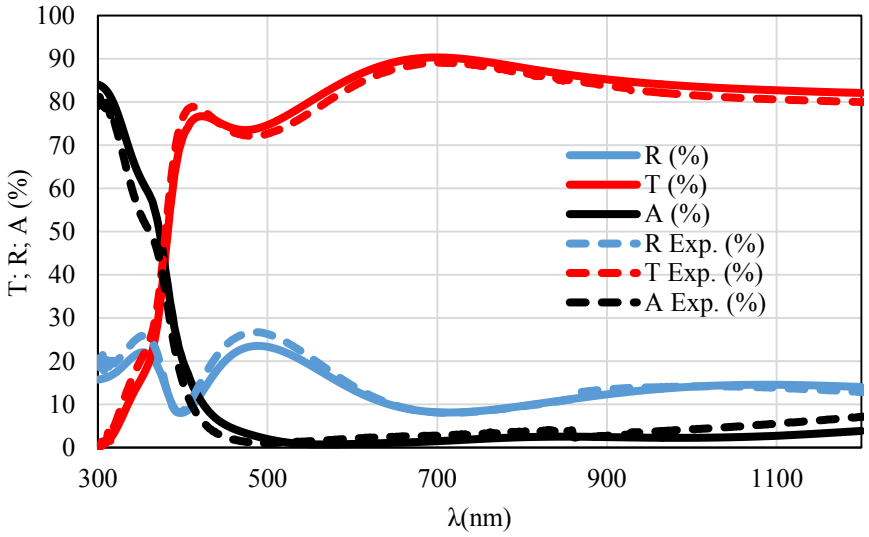


Figure 5.8: Simulated (solid) and experimental (dashed) R, T, and A for ITO/i-ZnO/SLG. The estimated thickness of ITO and i-ZnO is 147± 3nm and 50± 5nm respectively.

Chapter 6

RESULTS

In this chapter, the application and analysis of the electronic and optical characterization methods detailed in chapter 4 is presented.

6.1 Sample Preparation and Devices

The ACIGS devices were fabricated at the Institute of Energy Conversion following the standard procedure described in chapter 2. The ACIGS films were ~2.7 to 3 μm thick and the film composition was measured by energy dispersive x-ray spectroscopy (EDS). The films are slightly group I poor with a (Ag+Cu)/(In+Ga) ratio of ~0.8 - 0.9 as shown in table 6.1.

Table 6.1: Representative absorber film properties of devices studied. The bandgap as predicted from composition and as measured by QE is shown.

Sample Series (SS)	d (μm)	(Ag+Cu) /(In+Ga)	(Ag)/(Ag+Cu)	Ga/(In+Ga)	Eg (EDS)	Eg (QE)
D1	2.71	0.90	0.21	0.52	1.35	1.29
D2	3.25	0.82	0.27	0.57	1.39	1.31

The Ga fractions in the films ranged from 0.52 – 0.57 and the Ag ratios ranged from 0.21 – 0.27 yielding an optical bandgap, Eg, near 1.3 eV, although the bandgap determined from the film composition measured by EDS indicates a higher bandgap in both sample series (SS) D1 and D2.

The sample series, D1, was used to investigate the role of i-ZnO layer thickness while D2 was used to investigate the role of i-ZnO layer resistivity

determine from the sheet resistance. D1 and D2 represent samples from two separate deposition runs, where the absorber films were deposited by elemental source evaporation, with an unintentional variation in composition. Deposition conditions were nominally the same for both D1 and D2 absorbers. All samples in the same series were co-processed in the same CdS, ITO and Ni:Al grid runs to ensure uniformity in these layers and prevent run-to-run variation from affecting the results. The fabrication techniques and process variable required in varying the i-ZnO thickness and resistivity was described previously in chapters 2 whereas chapter 3 detailed related work published in literature.

6.1.1 Sample series D1 (effect of i-ZnO thickness)

To study the effect of i-ZnO thickness on device performance, five 1x1 inch pieces from the sample series D1 were selected and processed to finished devices, changing the thickness via the sputtering time of the i-ZnO layer for each piece while all other layers of the cell stack were identical. The details of the processing parameters are presented in table 6.2. The sheet resistance could not be measured by standard 4-point probe resistivity method.

Table 6.2: Sample set for i-ZnO thickness (t_{ZnO}) experiment with sample IDs, S1 to S5

Sample ID	**S1**	**S2**	**S3**	**S4** (Control)	**S5**
t_{ZnO} (nm)	0	10	30	50	100
R_{sh} (MΩ/□)	>1	>1	>1	>1	>1
N_{DZnO} (cm^{-3})	< 3E16	< 3E16	< 3E16	< 3E16	< 3E16

Attempts at measuring the sheet resistance of the thin-films on monitor SLG slides using Hall effect, were also unsuccessful as the films were too thin (< 100 nm) and the source-meter compliance limit could not provide the sensitivity required for the measurement. With an assumed electron mobility of 50 cm/V-s the resistivity was calculated from the sheet resistance and then the free carrier concentration was calculated ($\sigma = 1/\rho = \mu q N_{DZnO}$).

6.1.2 Sample series D2 (effect of AZO sheet resistivity)

To study the effect of AZO resistivity on device performance, three 1x1 inch pieces from the sample series D2 were selected and processes to finished devices, changing the resistivity of the i-ZnO layer for each piece while all other layers of the cell stack were identical. The details of the processing parameters are presented in table 6.3. The i-ZnO layer was replaced with an AZO layer. The thickness of AZO was maintained for all cells (S6 to S8) at 50 nm using a sputtering growth rate of ~8.5 nm/min and varying the Ar/O_2 ratio to vary the resistivity of the sputtered film as described in chapter 2. A fourth piece, S9, processed with the standard conditions was used as control.

Table 6.3: Sample set for ZnO resistivity (ρ) experiment with sample IDs, S6 to S8

Sample ID	**S6**	**S7**	**S8**	**S9** (Control)
R_{sh} (Ω/□)	800	35 K	138 K	>1 M (Control)
ρ (Ω-cm)	4.00E-03	1.75E-01	6.90E-01	1.00E+01
σ (S/cm)	250	5.71	1.45	0.10
N_{DZnO} (cm^{-3})	3.13E+19	7.14E+17	1.81E+17	1.25E+16

6.2 Current-Voltage Measurements and Diode Analysis

Figure 6.1 shows the solar cell parameters for the sample series D1.

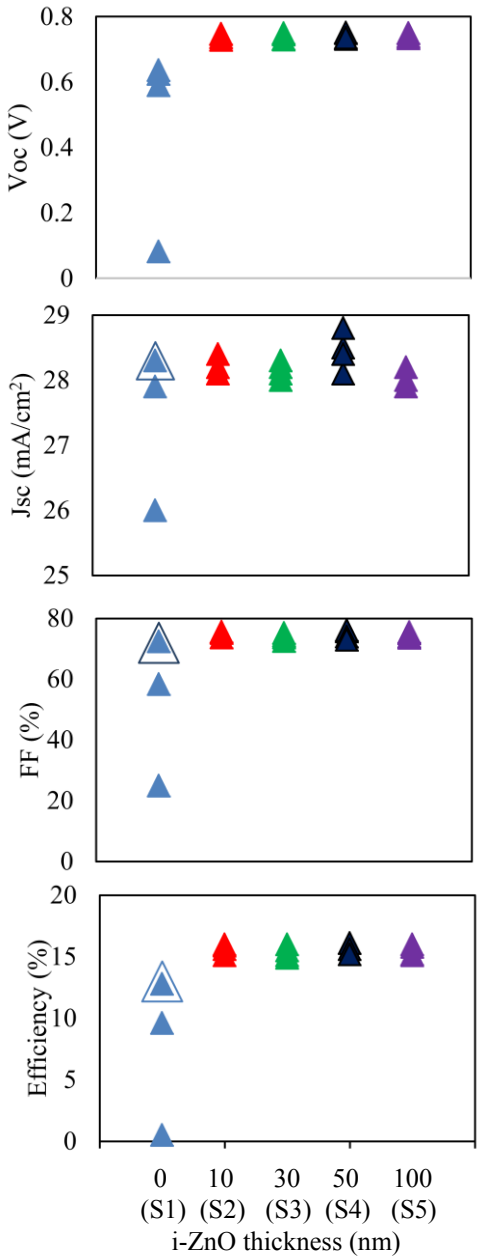


Figure 6.1: Device parameters for series D1(effect of i-ZnO thickness), showing samples (S1 to S5) and the cell parameters as a function of i-ZnO thickness

The device results for sample series D2 are presented in figure 6.2.

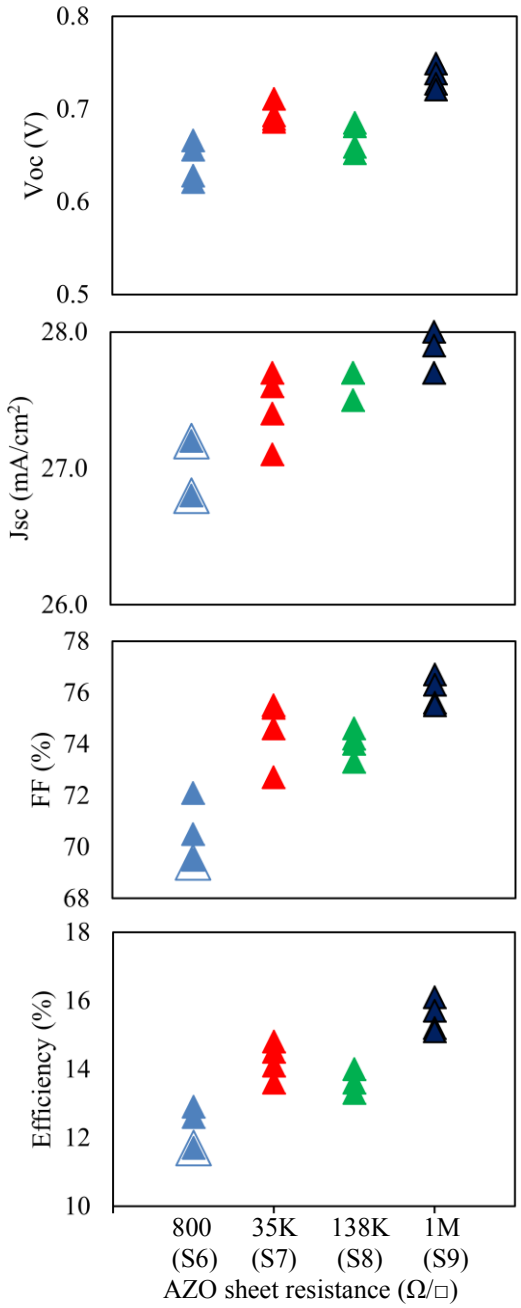


Figure 6.2: Device parameters for series D2 (effect of AZO resistivity), showing samples (S6 to S9) and the cell parameters as a function of AZO sheet resistance. Note the smaller scale for all parameters compared to figure 6.1.

From figure 6.1, while there is an obvious spread in S1 (0 nm), samples S2 to S5 have a very tight distribution for all parameters except for the J_{sc} of S4 which has a slightly larger spread.

In figure 6.2, one can identify an overall trend in device parameters with performance increasing as sheet resistance of the ZnO layer, except for S8. S7 tends to have a wider spread, but mostly has higher performance in most parameters compared to S8.

6.2.1 Diode analysis

Figure 6.3 is a representative plot of the four-step procedure.

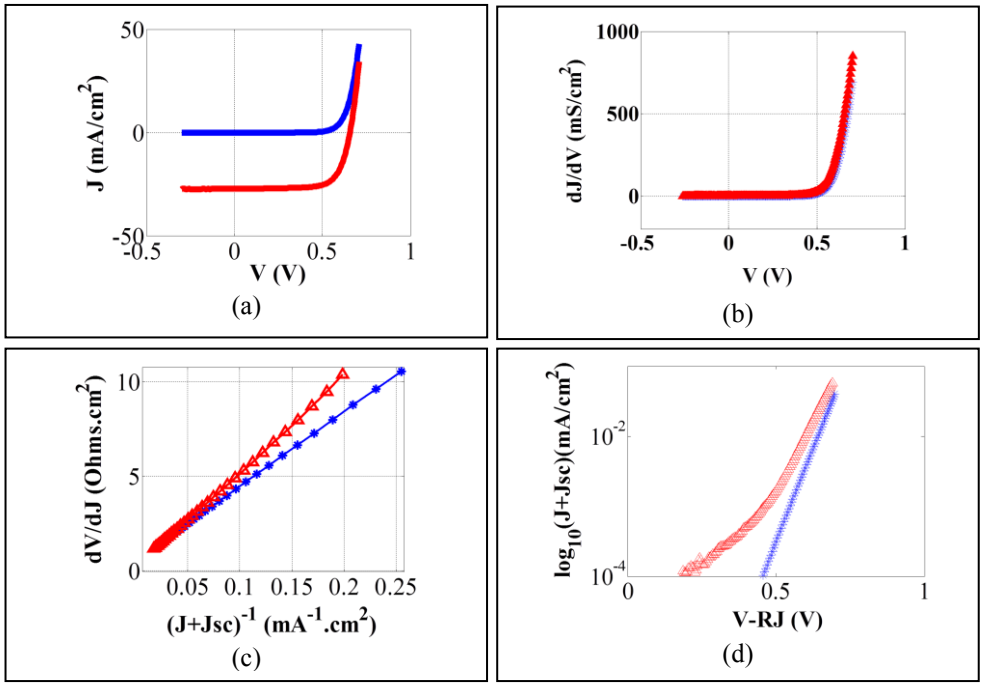


Figure 6.3: Diode analysis for ACIGS sample S2 (10 nm i-ZnO) (a) Light and dark JV characteristics (b) Shunt characterization (c) dV/dJ with fit to determine R_s and n_{id} (d) $\ln(J+J_{sc}-GV)$ vs. (V-RJ) to determine n_{id} and J_0. Data in blue is measured in the dark and data in the red under AM1.5 illumination

Highest efficiency cells were selected from samples S1 to S9. Assuming a lumped circuit approximation, circuit parameters were extracted using the diode analysis procedure described in chapter 4. The shunt conductance (G), the series resistance (R_s), the ideality factor (n_{id}) and the saturation current density (J_0) were extracted.

The measured JV parameters and the diode parameters derived from analyzing the JV raw data is presented in table 6.3.

Table 6.4: Device characteristics and diode parameters of solar cells in sample series D1 and D2. Two values of the parameters G, R_s, n_{id} and J_0 are reported for each cell. The first (upper value) is the parameter in the dark and the second (lower value) is the parameter under illumination

D1	**t_{ZnO} (nm)**	**Cell**	**Voc (mV)**	**Jsc (mA/ cm^2)**	**FF (%)**	**η (%)**	**G (mS/c m^2)**	**Rs (Ω-cm^2)**	**n_{id}**	**J_0 (mA/c m^2)**
S1	0	002	0.637	28.3	72.0	13.0	1.2E-1 5.6E-1	0.57 0.72	2.30 1.72	6E-5 1E-5
S2	10	001	0.747	28.4	75.5	16.0	2.5E-3 3.2E-1	0.63 0.40	1.38 1.78	1E-7 1E-6
S3	30	002	0.750	28.3	75.2	16.0	2.0E-1 2.5E-2	0.75 0.53	1.39 1.81	1E-7 3E-6
S4	50	001	0.750	28.5	75.7	16.1	2.3E-3 4.5E-1	0.48 0.31	1.42 1.78	1E-7 2E-6
S5	100	001	0.750	28.2	75.5	16.0	4.0E-3 8.6E-2	0.67 0.45	1.39 1.80	1E-7 2E-6
D2	**R_{sh} (Ω/□)**	**Cell**	**Voc (mV)**	**Jsc (mA/ cm^2)**	**FF (%)**	**η (%)**	**G (mS/c m^2)**	**Rs (Ω-cm^2)**	**n_{id}**	**J_0 (mA/c m^2)**
S6	800	001	0.656	27.2	72.1	12.9	4.4E-3 4.5E-1	0.50 0.24	1.56 1.97	2E-6 3E-5
S7	35K	002	0.711	27.6	75.4	14.8	8.6E-3 3.4E-1	0.60 0.65	1.76 1.72	2E-6 2E-6
S8	138K	001	0.685	27.5	74.2	14.0	3.5E-3 3.2E-1	0.41 0.58	1.99 1.79	1E-5 8E-6
S9	<1M	001	0.749	28.0	76.7	16.1	1.2E-2 3.5E-1	0.42 0.42	1.61 1.66	6E-7 1E-6

It is assumed that the series resistance, shunt conductance and the light generated current are independent of voltage and light intensity. However, for most of the devices, the plot of dJ/dV shows very slight voltage dependence under illumination. This is most clearly seen from the value of G in the light being much higher than G in the dark. Since G is the slope at short circuit, the higher slope indicates a slight voltage dependence for photocurrent collection as supported by the QE spectra Discrepancy between the light and dark data reduces the accuracy of determining G, R_s, n_{id} and J_0. Forcing a linear fit on the dV/dJ plot resulted in diode ideality factors between 1 and 2 for most cells, with the exception of S1, which has an ideality factor greater than 2. Generally, the ideality factor increases under illumination.

A close observation of samples in series D2 shows that the change in the AZO sheet resistance over three orders of magnitude has no significant effect on the series resistance. No clear trend is observed, perhaps due to the fact that the AZO layer is very thin relative to the area. The thickness of the AZO layer is ~50 nm and all the other dimensions are several orders of magnitude greater, thus the AZO layer has a small aspect ratio. The RMS roughness of the CIGS surface has been estimated to be ~50 – 100 nm [29]. Perhaps the combination of the CdS and ZnO deposited over the absorber surface conforms to the surface roughness and may not necessarily a continuous film across the surface.

For sample S1, with no ZnO, the diode saturation current, J_0, in the light and dark is several times larger than all other samples except S8. This may explain the drop in V_{oc} due to higher recombination occurring in the device via weak diodes and shunts. The high resistance ZnO layer may prevent these inhomogeneity from dominating the V_{oc}.

6.3 Quantum Efficiency Measurements

QE measurements taken for all samples in series D1 is presented in figure 6.4 below, where d(QE-S*)/dL is the derivative of the QE with respect to wavelength used to determine the optical bandgap of the absorber (see table 6.1 for bandgap values)

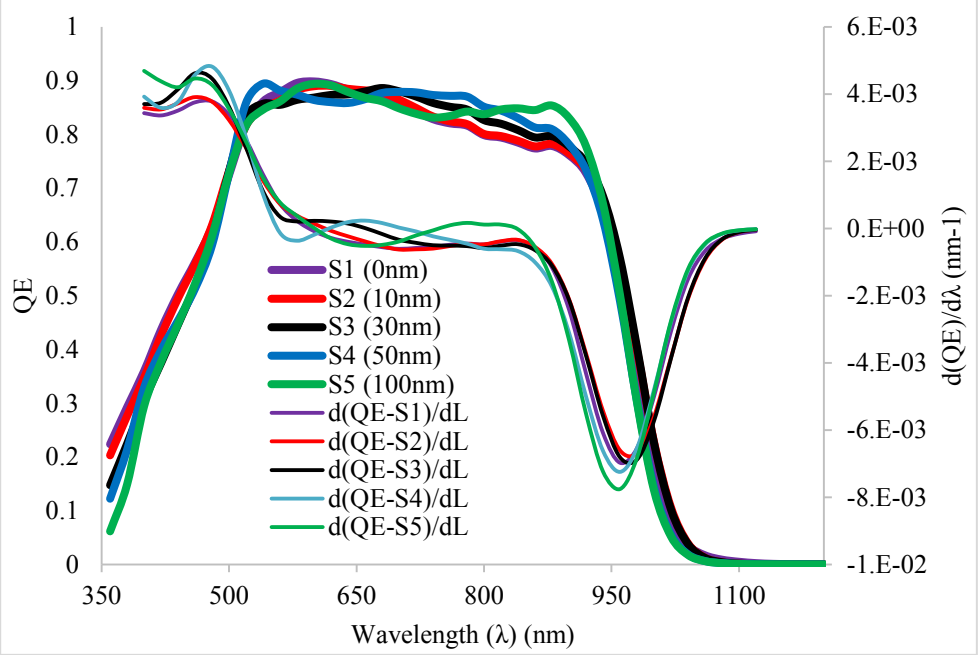


Figure 6.4: QE measurements (thicker lines) for series D1, with varying i-ZnO thickness, 0, 10, 30, 50, and 100 nm. The derivative plot (thinner lines) shown on the secondary axis is used to determine the optical bandgap of the absorber from the minimum around 960 nm.

The integrated QE (IQE) is presented in table 6.5 below and compares well with the J_{sc} measured from JV measurements. The QE measurements at -1 V bias (not shown) is slightly higher in the long wavelength region compared to the QE at 0 V bias indicating that there is a small amount of incomplete collection in the devices but this loss is insignificant.

Table 6.5: IQE and J_{sc} for sample series D1 and D2

	S1	S2	S3	S4	S5	S6	S7	S8	S9
IQE	27.9	28.1	28.1	28.0	27.9	27.2	27.5	27.5	28.0
J_{sc}	28.3	28.4	28.3	28.5	28.2	27.2	27.6	27.5	28.0

The QE measurements for sample series D2 is presented in figure 6.5.

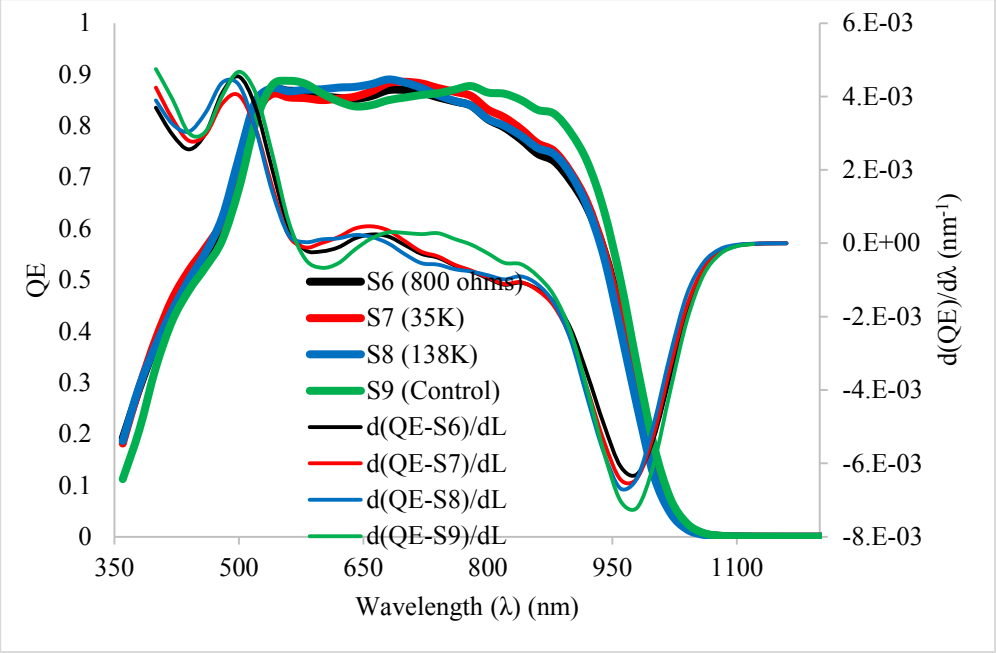


Figure 6.5: QE measurements for samples series D2. The i-ZnO layer was replaced with AZO and O2 was adding in the sputtering process to vary the resistivity of the AZO film (800, 35 K, 138 K Ω/□).The derivative plot shown on the secondary axis is used to determine the optical bandgap of the absorber.

All samples with AZO have similar features in the QE spectra, the most obvious being a steady decrease in QE toward long wavelength unlike the control. Measurements of QE under -1 V bias (not shown) indicated gave QE with a slightly

higher response at long wavelengths, indicating collection was slightly voltage dependent.

6.4 Results of Defect Density and Carrier Concentration Measurements Using AS and DLCP

Representative samples from sample series D1, samples S2 (10 nm i-ZnO) and S5 (100nm i-ZnO) were characterized using AS and DLCP. Measurements using these techniques were not successful for sample series D2; perhaps due to a depleted/intrinsic absorber layer (geometric capacitance) or that the samples were "leaky" due to a poor capacitor model established at the junction [47]. The devices in series D2 did not show a change in capacitance as a function of temperature or frequency.

6.4.1 Admittance spectroscopy (AS)

In this section results and analysis of capacitance measured as a function of frequency (100 Hz to 1 MHz) and temperature (113 K to 293 K) is presented. Results and analysis for S2 are shown in figure 6.6. The objective was to determine the defect activation energy, (E_a), attempt-to-escape frequency, υ_0, (which is related to the capture cross-section as, $\upsilon_0 = N_{V,C}\langle v_{th}\rangle\sigma_{h,e}$) and the defect density distribution as a function energy. The measurement was affected by noise at low frequencies (close to 100 Hz). This lack of sensitivity limits the ability to probe deep defects. Samples were leaky and hence no useful information could be extracted from the conductance data. The derivative of the capacitance was noisy as shown in figure 6.6b. This makes it difficult to accurately identify the maxima and thus the peak frequencies necessary to determine E_a and υ_0 in figure 6.6c. However, the E_a was estimated to be ~41 meV and the attempt-to-escape frequency was estimated to be 1E6 s^{-1}. Although there is not

much work in the literature reporting AS characterization of ACIGS devices, CIGS absorbers have been characterized in great detail.

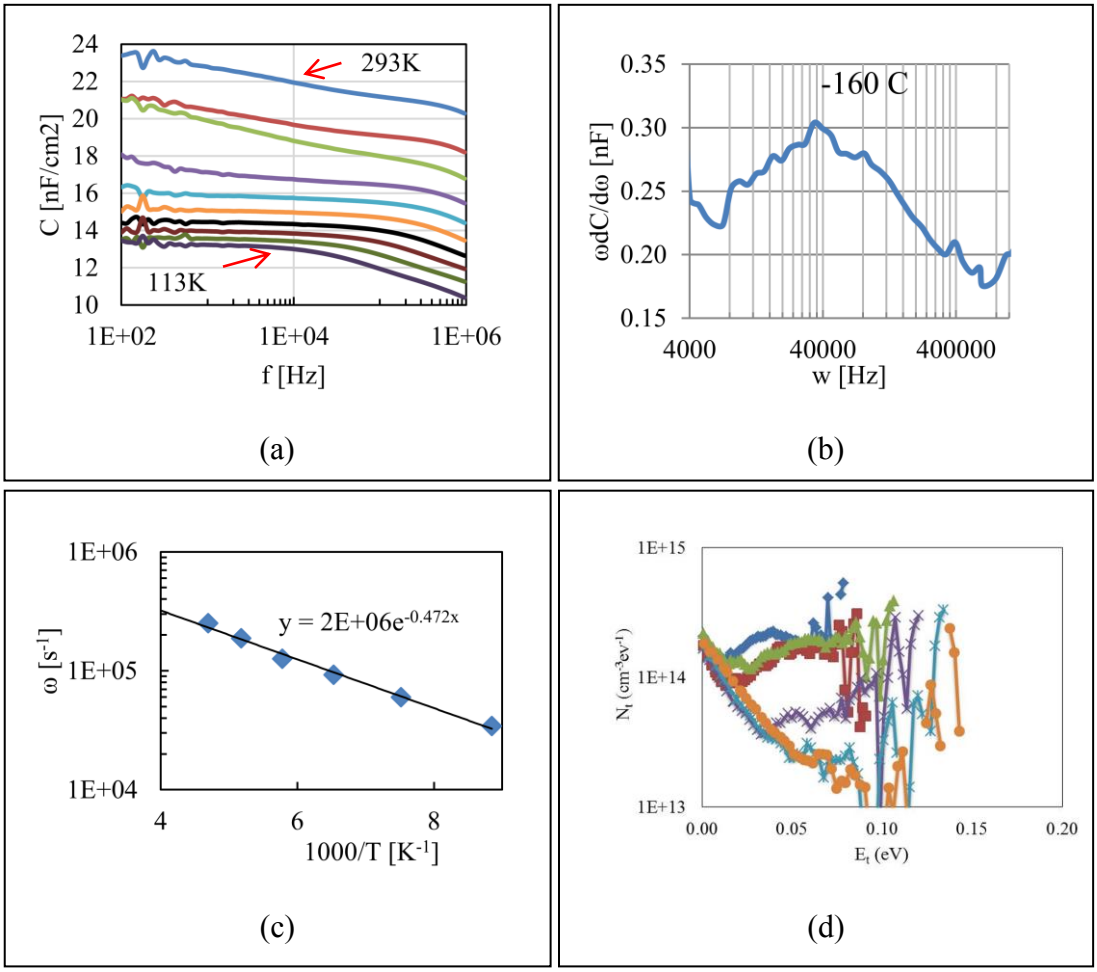


Figure 6.6: (a) Sample AS raw data (C [nF] vs. f [Hz]) for sample S2 taken in 20K increments from 113 to 293 K (b) Representative derivative of capacitance ishowing characteristic (peak) frequency at 113 K (c) Arrhenius plot of peak frequency giving E_a and υ_0 from slope and intercept respectively (d) Defect density vs. energy at different temperatures

Walter et al [44] , reports an E_a of 310 meV and υ_0 of 1.1E12 s^{-1}, Herberholz et al [45] , report an E_a of 123 and 280 meV which they identify as the N1 and N2 defects respectively and a pre-exponential factor of 2E6 $s^{-1}K^{-1}$, Jian et al [46], report an E_a of 268 meV and υ_0 of 4E12 s^{-1}. Finally Erslev et al [23] reported 150 to 250 meV for ACIGS devices. However measurements on ACIGS devices at IEC show Ea in the range, 40 to 100 meV and υ_0 in the range 1E6 to 1E9 s^{-1}. Noise in the capacitance data causes a temperature dependent shift and scatter in the defect density of states determination, making it difficult to identify the density and the energetic position of defects.

Sample S5 had a relatively flatter AS response compared to S2 but the measurement stilled suffered from noise at low frequency and resonance at high frequency. Figure 6.7 shows the measurement and analysis.

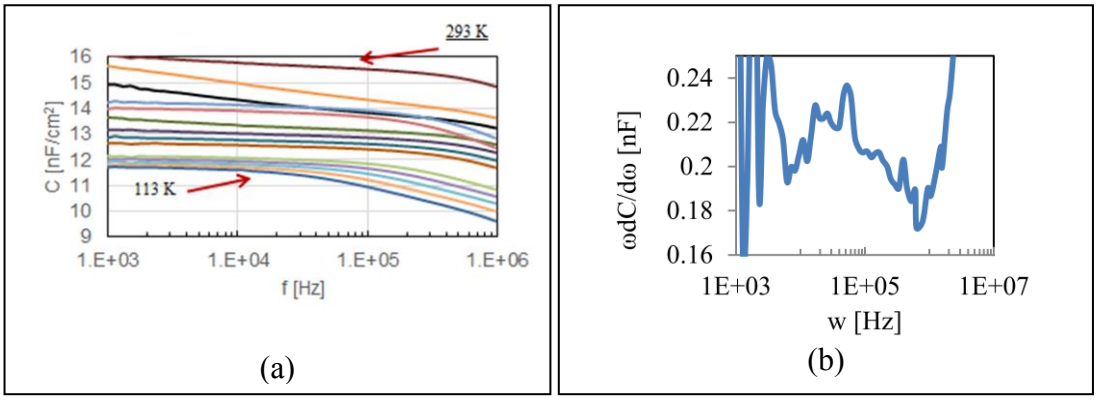


Figure 6.7: (a) C vs. f at T from same range as Figure 6.6 for sample S5 (100 nm i-ZnO). No distinct capacitance step observed (b) Representative plot showing noisy derivative at 113 K.

6.4.2 Results from Mott-Schottky (MS) analysis and drive level capacitance profiling (DLCP)

The defect responses measured by DLCP depends on the probing energy determined by the measurement frequency and temperature. Figure 6.8 shows results from DLCP and MS analysis of sample S2.

In the MS analysis measures all charges that can respond across the entire device. Both interface and deep states can respond. DLCP on the other hand is immune to interface states. A comparison of the DLCP and MS profiles at 113 K for S2 as shown in figure 6.8, indicates defect density > 1.6E15 cm^{-3}. The free carrier density estimated from the DLCP at 113 K is ~8.6E14 cm^{-3}.The depletion width estimated from the measurement of the capacitance at 0 V bias and a temperature of 298 K is ~0.46 μm. The depletion width, free carrier concentration and defect density extracted for S5 is 0.52 μm, 5.84E14 cm^{-3} and 2.4E15 cm^{-3} respectively.

Given the noise in the data reduction, we feel these values are the same within experimental error indicating that the i-ZnO thickness had no effect on junction charge or defect density, as expected. This observation is in agreement with SCAPS modeling presented in chapter 5. The modeling predicts that i-ZnO thickness does not affect the electrical properties junction.

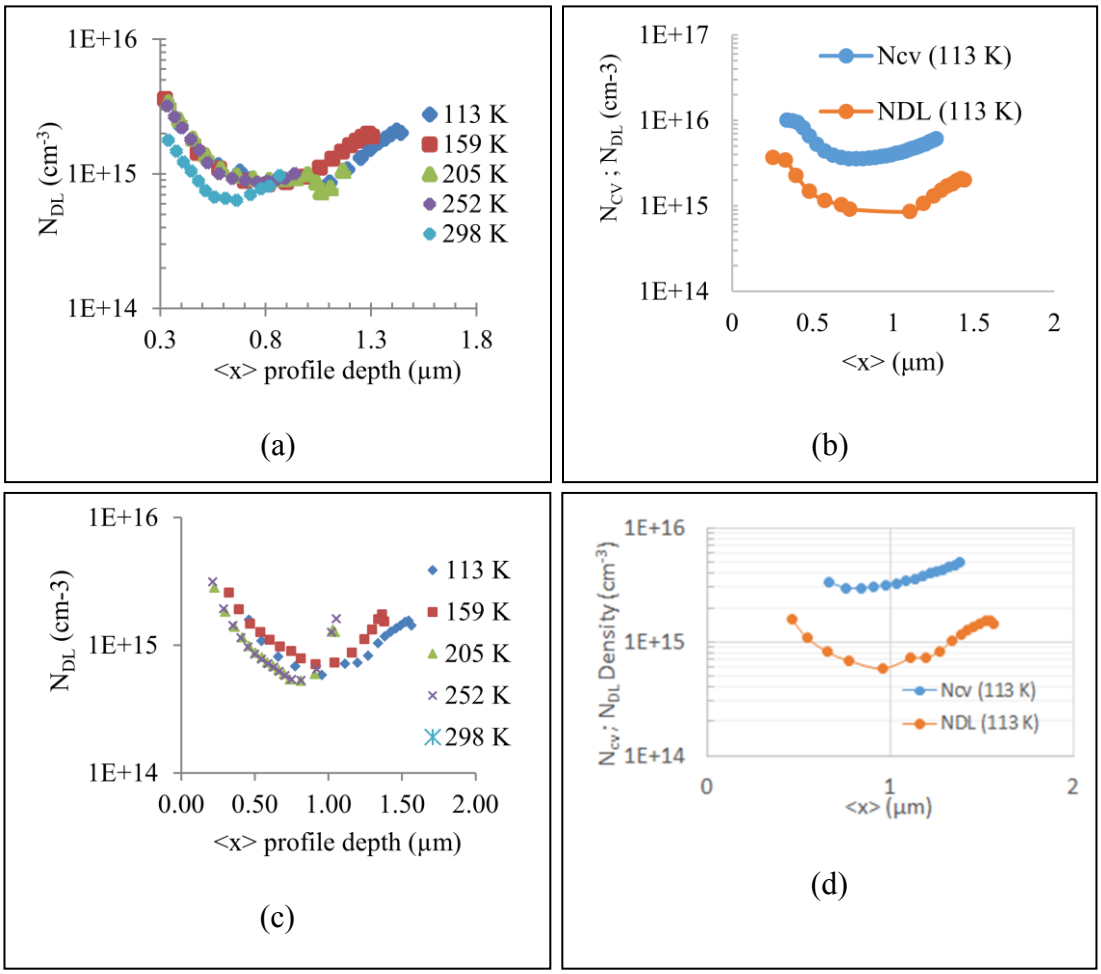
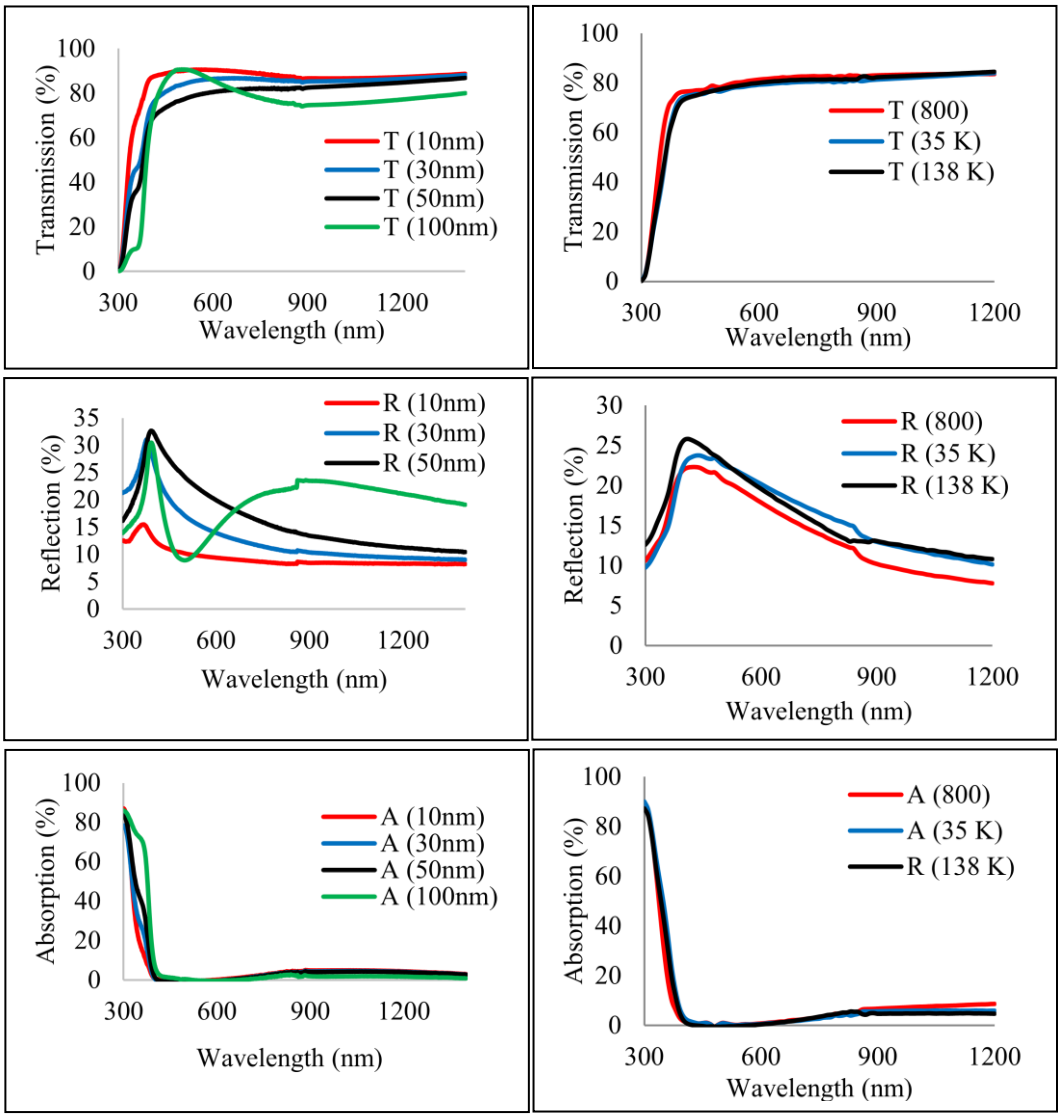


Figure 6.8: (a) DLCP profiles at different temperatures for S2 (10 nm i-ZnO) (b) Comparing MS and DLCP profiles at low temperature (113 K) for S2 (c) DLCP profiles at different temperatures for S5 (100 nm i-ZnO) (d) Comparing MS and DLCP profiles at low temperature (113 K) for S5

6.5 Results of Transmission and Reflection (T&R) Measurements

This section details the results of the transmission and reflection measurements of the i-ZnO and AZO films used in sample series D1 and D2 respectively. The films were deposited on soda-lime glass (SLG) monitor slides during the sputtering process. For the series D1, transmission increases with decreasing thickness as expected, with a corresponding decrease in absorption as shown in figure 6.9. However the differences in the absorption as a result of changing the film thickness does not lead to an observed trend in J_{sc} of the finished devices as small changes in absorption are negligible when the film is sandwiched in the solar cell stack. There is no significant difference in the absorption and transmission of the AZO in sample series D2.



(a) (b)

Figure 6.9: T&R measurements and calculated absorption, A, for (a) i-ZnO of thickness 0, 10, 30, 50 and 100 nm (b) AZO of thickness 50 nm and sheet resistance, 800, 35 K and 138 KΩ/□. The absorption was calculated as A = 100-T-R.

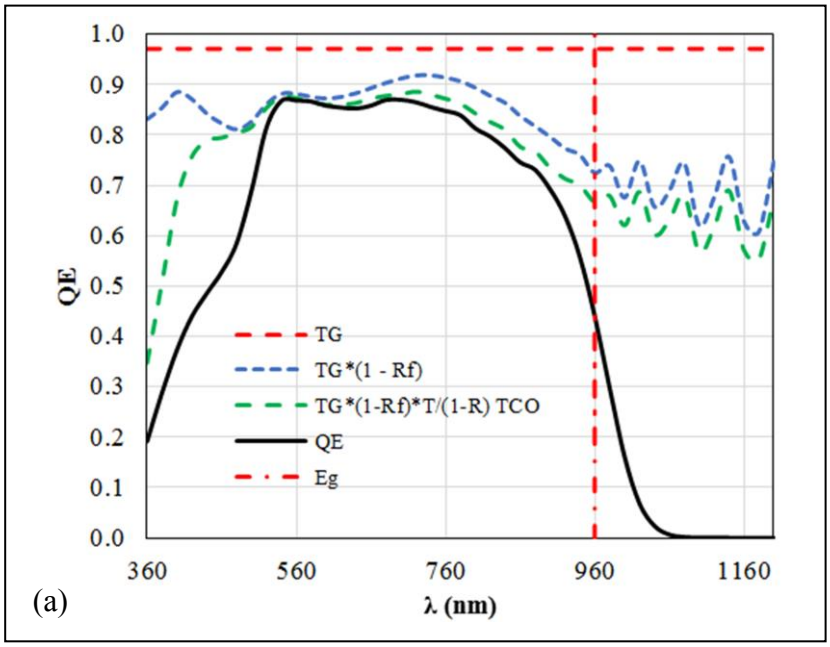
6.6 Optical Loss Accounting and Correction

The loss analysis consists of 2 cells (best and worst cells in terms of efficiency) selected from sample series D2 in table 6.4. The cells are S6 and S9.

Optical losses in the solar cell due to grid shadowing (T_G), front reflection, (R_f), TCO absorption, CdS absorption, incomplete generation and incomplete collection are detailed below. The method combines QE and T&R measurements and is described in chapter 4. A representative analysis of sample S6 is shown below in figure 6.10. The QE plots shown in figure 6.10b are cumulative corrections applied to the actual QE measurement (blue line) after accounting for the various losses. Removing the known losses increases the QE to nearly unity as expected in the range 500-950 nm indicating negligible unaccounted losses. The low QE below 550 nm is due to CdS absorption. Corrections for the absorption in CdS are not applied to the QE in figure 6.10. However it is quantified by finding the available current in the wavelength range 360 to 540 and subtracting the value of the integrated current in the same wavelength range, after all other losses have been accounted for.

Table 6.6 shows values of the current losses for samples series D1 and D2 (bandgap = 1.29eV). The total available current density, J_{tot}, for this bandgap is 35.44 mA/cm^2.

The separation of optical losses into its constituents is as depicted in table 6.6 enables the identification of the best opportunity for improvements in the solar cell stack. Typically, record devices have an ARC coating that significantly reduces the front reflection. In such devices, the largest optical loss arises from absorption in the CdS.



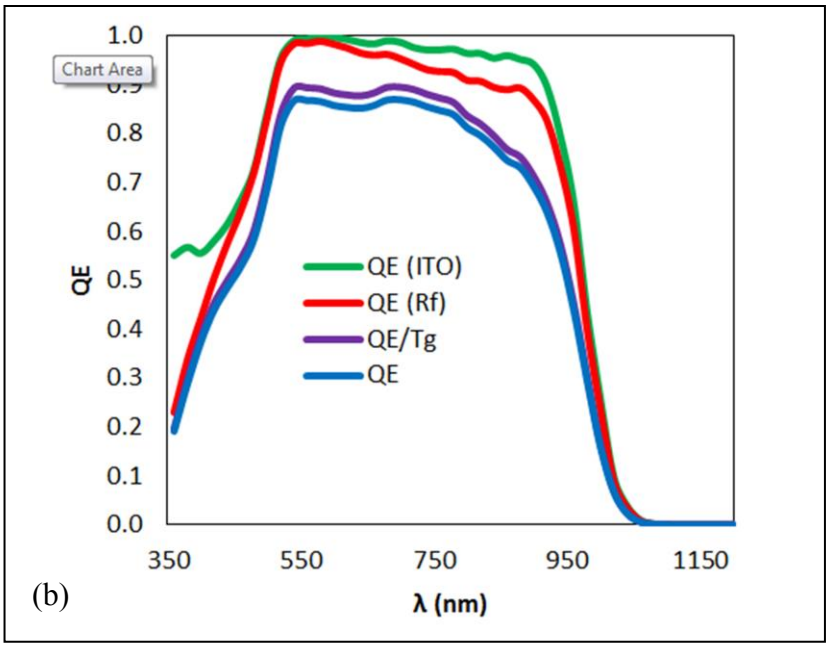


Figure 6.10: (a) Optical loss breakdown (b) Cumulative correction to QE

Table 6.6: Photocurrent losses in the ACIGS solar cell stack

Optical loss mechanism	**Current loss , ΔJ (mA/cm^2)**		**Percentage loss $\Delta J/J_{tot}$(%)**	
	S6	S9	S6	S9
Grid shadowing	0.81	0.82	2.22	2.32
Front reflection	3.52	3.27	9.66	9.24
Absorption in ITO	1.59	1.60	4.36	4.51
Absorption in CdS	1.82	2.09	4.99	5.91
Incomplete generation	0.83	0.64	2.29	1.79

Chapter 7

CONCLUSIONS AND FUTURE WORK

Electrical and optical characterization methods have been used to study ACIGS devices in order to extract useful information about the device operation and limiting loss mechanisms affecting device performance. The electrical and optical characterization techniques employed included JV, QE, CV, AS, DLCP, VASE and UV-VIS. The devices were fabricated using techniques which included, glass cleaning, Mo sputtering, co-evaporation of ACIGS, CBD of CdS, sputtering of i-ZnO and ITO and e-beam evaporation of Ni-Al grids. Devices on 1x1 inch SLG substates were isolated by scribing.

The central focus of this thesis was to study the role of the i-ZnO layer in the standard solar cell structure (SLG/Mo/ACIGS/CdS/i-ZnO/ITO/Ni-Al). Two experiments were conducted: first, the thickness of the i-ZnO was varied by varying the sputtering time and in the second, the i-ZnO was replaced with AZO, and the resistivity of the AZO was changed by adding O_2 to the film during the sputtering process.

7.1 Effect of i-ZnO Thickness on Device Performance

The historical evolution of the i-ZnO in the CIGS solar cell structure was covered in chapter 3. The role of the i-ZnO has interested researchers over the years and was a major motivation for this research effort. This research has shown that the effect of the thickness of the i-ZnO layer on the overall device performance is

negligible and no clear trend can be identified for thicknesses ranging from 10 nm to 100 nm. However, devices fabricated by omitting the i-ZnO showed a larger spread in device parameters and in general, showed a decrease mainly in V_{oc}. Devices with no i-ZnO layer had much higher G and J_0 compared to all other devices. It would appear that depending on the homogeneity and surface roughness of the CdS/ACIGS surface, an even much thinner layer than the standard 50nm could be used without negatively affecting device performance. It may be even more important to optimize the i-ZnO and ITO combined thickness for their anti-reflective properties than trying to optimize the i-Zno alone. Furthermore, optical loss analysis showed that the absorption due to the TCO layer could be optimized; however, there is not much gain to be made in terms of current. This suggests that optimizing the window layer optical function may be of minor importance and that emphasis should be placed on the absorber growth, to provide a better path to device improvements. FF of the devices is shown to be independent of i-ZnO layer thickness for the thickness range studied.

7.2 Effect of AZO Resistivity on Device Performance

The resistivity (and thus the doping concentration) of the AZO layer was changed by three orders of magnitude from, 4E-3 to 1E1 Ω-cm (~1.25E16 cm^{-3} to 3.13E19 cm^{-3}). It was expected that the conductivity of the AZO would have an effect on the electric field distribution across the junction, especially if the CdS was fully depleted. Device results indicated a relatively small but monotonic decrease in device parameters as the resistivity of the AZO was reduced. Overall, the spread in device parameters was smaller in this experiment than with the thickness variation experiment. Changing the resistivity over 3 orders of magnitude did not have a significant effect on the overall series resistance of the device; this may be due to the

fact that the series resistance is dominated by the ITO, absorber/buffer and contact resistance. Perhaps the small aspect ratio of the ZnO layer and the surface roughness of the conformal CdS on CIGS may introduce discontinuities across the film, so that the effective resistance is reduced.

In devices from both experiments, the ideality factors for the devices ranged from 1.5 to 2.0 indicating that devices are dominated by SRH recombination.

It would appear that, higher performing devices require a high i-ZnO resistance. Recently some researchers [68] have suggested that the addition of O_2 during the i-ZnO sputtering process may have some beneficial effects on junction properties. They propose that addition of 2% O_2 reduced the absorption loss of the overlaying transparent conductor and improved the electronic properties of the underlying CdS/CIGS heterojunction. Defect passivation, increased free carrier density and diffusion length is attributed to the increased distribution of Na around the heterojucntion due to plasma-activated oxygen. This effect was not observed with the AZO experiment where up to 2% O2 was added to vary the resistivity of the film. Oxygen is not added in standard i-ZnO deposition process at the IEC.

7.3 Capacitance Measurements

From capacitance measurements at room temperature and 0 V bias, a depletion width of 0.52 μm and absorber free carrier density of 5.84E14 cm^{-3} was measured for a sample that had i-ZnO thickness 100 nm. For another sample with i-ZnO thickness of 10 nm, the depletion width and free carrier density were 0.46 μm and 8.6E14 cm^{-3} respectively. Given the noise in the data reduction, we feel these values are the same within experimental error indicating that the i-ZnO thickness had no effect on junction charge or defect density, as expected. This observation is in agreement with SCAPS

modeling presented in chapter 5. The depletion width measured from capacitance (MS) suggests that the CdS deposited by CBD at the IEC may not be as highly doped compared to those reported in literature. Burgelman and Gloeckler report CdS free carrier density of 1E17 and 1.1E18 cm^{-3} respectively.

It is generally accepted that the CdS is fully depleted. Hence using the equation relating charge density on both sides of a p-n junction,

$$N_A X_A = N_D t_{CdS} \tag{7.1}$$

the value of the CdS free carrier concentration, N_D, is estimated to be in the range 6E15 to 8E15 cm^{-3}.

Defect activation energies of 41 and 75 meV and attempt to escape frequency of 1E6 and 4.5E7 s^{-1} was measured for two different films the same sample series.

7.4 Comparison of Simulated and Experimental Results

The simulation of the effect of ZnO thickness and resistivity change in IEC CIGS and ACIGS devices presented in chapter 4, suggests that there is no effect electrical performance of finished devices. A decrease in J_{sc} due to absorption is however observed as the thickness of the i-ZnO is increased beyond 200 nm. In fabricated devices, there seems to be a weak trend with device performance as all parameters seem to increase with the ZnO resistivity. This is in disagreement with the simulation results.

The simulations may not adequately represent the exact physical and optical effects that i-ZnO encounters in a practical device. While the 1D simulation predict no impact of the i-ZnO even when it is absent, in real devices it serves an important role in reducing the variation in performance especially V_{oc}, due to non-ideal spatial

variations in junction potential or other shunting mechanisms not predicted in 1D models

7.5 Optical Loss Analysis

Identifying and quantifying the optical losses in typical ACIGS/CdS solar cells has been presented. A breakdown of the optical losses into its constituents, suggests that efforts should be focused on minimizing absorption losses in the CdS buffer layer. The total current losses due to optical losses are on the order of 8.5 mA/cm^2. This represents a total percentage loss, $\Delta J/J_{tot}$, of ~24%, at a bandgap of 1.3 eV, without an ARC layer. An ARC as applied to record devices could reduce this loss to ~16 – 17%.

7.6 The ACIGS Absorber

Solar cells made from Ag alloyed CIGS tend to be well behaved under in the dark and under illumination, having only slight in n_{id}, G and Rs under illumination. QE measurements under reverse bias are almost exactly superimposed on QE measured at 0 V bias, suggesting that there is little or no voltage dependent collection and that the solar cells fabricated at the IEC behave as expected with no evident surface barriers or misalignment that could generally lead to very poor devices at least at room temperature and above.

7.7 Further Studies

The relatively low free carrier density of ACIGS devices (compared to CIGS) and its effect on junction properties like the depletion width, built-in potential and electric field distribution may be worth investigating. SCAPS simulations suggest a significant increase in V_{oc} with increasing absorber doping density. The simulations also suggest that changes to the i-Zno layer, may have a greater effect when the

absorber carrier density greater than or equal 1E16 cm^{-3}. The modeling suggests that an efficiency gain of 1% is possible by changing the i-ZnO properties.

The role of adding O_2 in i-ZnO sputtering process may be worth investigating. A trend in the overall device performance is seen with varying the resistance of the AZO layer, perhaps addition of oxygen to the i-ZnO sputtering process may be important for device performance as recently reported [68].

More fundamental understanding of the absorber material and device operation is required. A clear path to increased Voc would be to significantly reduce, recombination in grain boundaries, interfaces, surfaces and the bulk as well as increased hole density and minority carrier lifetime. The complexity of the material system, device stack and mechanisms controlling these parameters suggests that the task of multilayer polycrystalline thin film solar cell device optimization is not trivial.

REFERENCES

1. M. Green. 1982. "Solar Cells: Operating Principles, Technology, and System Applications, Chapter 1, Prentice Hall, Englewood Cliffs, NJ, 1 - 12

2. W. Shockley and H. J. Queisser. 1961. "Detailed Balance Limit of Efficiency of p-n Junction Solar Cells" J. Appl. Phys. 32, 510

3. D. Abou-Ras, T. Kirchartz, and U. Rau (Eds.), 2011. "Advanced Characterization Techniques for Thin Film Solar Cells", Wiley-VCH

4. T. Nakada and T. Takahiro, 2001. High efficiency superstrate type CIGS thin film solar cells with graded bandgap absorber layers Proc. 17th Euro. Photovolt. Sol. Energy Conf., Munich

5. A. Luque. and S. Hegedus (Eds), 2011. "Handbook of Photovoltaic Science and Engineering", 2nd Ed. Wiley

6. Rau U., Taretto K., and Siebentritt S., 2009. Grain Boundaries in CIGS Thin-film Solar Cells. Appl. Phys. A, 96, 221 – 234

7. S. Siebentritt. 2002. "Wide gap chalcopyrites: material properties and solar cells". Thin Solid Films 403 –404. 1–8

8. I. Repins, M. Contreras, M. Romero, Y. Yan, W. Metzger, J. Li, S. Johnston, B. Egaas, C. DeHart, and J. Scharf, 2008 "Characterization of 19.9%-Efficient CIGS Absorbers." 33rd IEEE Photovoltaic Specialists Conference

9. P. Jackson et al, 2011. "New World Record Efficiency for CIGS thin-film Solar Cells beyond 20%". Prog. Photovolt. Res. Appl. 19: 894-897

10. PV magazine, http://www.pv-magazine.com/news/details/beitrag/zsw-sets-217-thin-film-efficiency-record_100016505/#axzz3J1ONNQNQ. September 22, 2014

11. Green, Martin A., Emery Keith, Hishikawa Yoshihiro, Warta Wilhelm, Dunlop Ewan D., 2013. Solar cell efficiency tables (version 42) Prog. Photovolt: Res. Appl.Vol. 22, Issu. 1, pp. 1 - 9

12. H. S. Ullal, K. Zweibel and B. V. Roedern. 1997. "Current Status of Polycrystalline Thin Film PV Technologies". Proceedings of 26th IEEE Photovoltaic Specialist Conference, Sept. 28 - Oct. 03, Anaheim, California, pp: 301

13. A. Jasenek, U. Rau, K. Weinert, I. M. Kotschua and G. Hanna et al. 2001. "Radiation Resistance of Cu(InGa)Se2 Solar Cells Under 1 MeV Electron Irradiation". Thin Solid Films, 387: 228-230

14. Rui Kamada, William N. Shafarman, and Robert W. Birkmire. 2010. " $Cu(In,Ga)Se_2$ Film Formation from Selenization of Mixed Metal/Metal-Selenide Precursors". 94. 3, Elsevier, pp. 451-456

15. S. H. Wei, S.B. Zhang and A. Zunger. 1999. “Effects of Na on the electrical and structural properties of CuInSe2,” J. Appl. Phys. 85, 7214-7218.

16. D. K. Schroeder. and A. A. Rockett. 1997. "Electronic effects of sodium in epitaxial CuIn1-xGax Se2". J. Appl. Phys. 82, 10: 4982 - 4985

17. Binsma, J.J.M. and Van der Linden, H.A. (1982) Preparation of thin $CuInSe_2$ films via a two-stage process. Thin Solid Film, 97, 237–243

18. Mickelsen, R.A. and Chen, W.S. (1980) High photocurrent polycrystalline thin film CdS/CuInSe2 solar cell. Appl. Phys. Lett., 36, 371–373

19. Gabor, A.M., Tuttle, J.R., Albin, D.S., Contreras, M.A., Noufi, R., Jensen, D.G., and Hermann, A.M. (1994) High efficiency $CuIn_xGa_{1-x}Se$ solar cells from $(In_xGa_{1-x})_2Se_3$ precursors. Appl. Phys. Lett., 65, 198–200.

20. S. Siebentritt, U. Rau, Wide-Gap Chalcopyrites. Springer. Berlin. (2006)

21. Mickelsen R, Chen W, Proc. 15th IEEE Photovoltaic Specialist Conf., pp 800–804 (1981).

22. Boyle, J. H. and McCandless, B. E. and Shafarman, W. N. and Birkmire, R. W., 2014. “Structural and optical properties of (Ag,Cu)(In,Ga)Se2 polycrystalline thin film alloys”, J. of Appl. Phys., 115, 223504

23. Pete T. Erslev, G. Hankett, W. N. Shafarman, J.D. Cohen, 2009. “Characterizing the effects of silver alloying in chalcopyrite CIGS solar cells with junction capacitance methods. Mater. Res. Soc. Synp. Proc. Vol. 1165

24. J. D. Cohen, J. T. heath and W. N. Shafarman, 2003. New junction capacitance methods for the study of defect distributions and carrier properties in the copper indium diselenide alloys. Mater. Res. Soc. Symp. Proc. Vol. 763

25. W. Chen et al., in Proc. 19th IEEE Photovoltaic Specialist Conf. (1987), pp. 1445–1447

26. R. Potter, Sol. Cells 16, 521–527 (1986)

27. Potter R, Eberspacher C, Fabick L, Proc. 18th IEEE Photovoltaic Specialist Conf., 1659–1664 (1985).

28. Mitchell K, Liu H, Proc. 20th IEEE Photovoltaic Specialist Conf., 1461–1468 (1988).

29. W. N. Shafarman; R. S. Huang; S. H. Stephens; 2006, "Characterization of Cu(InGa)Se2 Solar Cells using Etched Absorber Layers," Photovoltaic Energy Conversion, Conference vol.1, no., pp.420-423

30. Kessler, J., Wiedeman, S., Russell, L., Fogleboch, J., Skibo, S., Arya, R., Carlson, D., 1996. "Front contact optimization for Cu(In,Ga)Se2 (sub)modules," Photovolt. Spec. Conf., Conference Record of the Twenty Fifth IEEE, pp.885,888

31. J. Kessler, J. Norling, O. Lundberg, J. Wenneberg, L.Stolt, 2000. "Optimization of RF-sputtered ZnO/ZnO:Al for CIGS based devices", 16th European photovolt. Sol. Energy Conf.

32. U. Rau and M. Schmidt, 2001; "Electronic Properties of ZnO/CdS/CIGS Solar Cells - aspects of Heterojunction Formation". Thin solid films, Vol.387, Iss. 1-2, pp 141 - 146

33. M. Ruckh, D. Hariskos, U. Rühle, H.W. Schock, R. Menner, B. Dimmler, 1996. "Applications of ZnO in CIGS Solar Cells", in Proceedings of the 25th IEEE Photovoltaic Specialists Conference, p.825

34. F.S. Hasoon, X. Li, A. Kanevce, C. Perkins, and S. Asher, H.A. Al-Thani 2008; "Investigation of the Effect of i-ZnO Window Layer on the Device Performance of the Cd-Free CIGS Based Solar Cells", Photovoltaic Specialists Conference, 33rd IEEE

35. Scheer, R.Messmann-Vera, L.Klenk, R. Schock, H.-W., 2011. "On the role of non-doped ZnO in CIGSe solar cells", Photovolt: Res. Appl.20 Issu.6 pp.619-624

36. C. Köble, D. Greiner, J. Klaer, I. Lauermann, R. Klenk, 2009. "The Role of Undoped ZnO in CuInSe2 Based Thin Film Solar Modules", 24th Euro. Photovolt. Sol. Energy Conf. pp. 2924

37. K. Ramanathan, J. Keane, R. Noufi, 2005, in Proceedings of the 31st IEEE Photovoltaic Specialist Conference, p.195 Solar Energy Conference, 2000, p.775

38. McCandless and S.S. Hegedus, 1992. "Influence of CdS Window Layers on Thin Film CdS/CdTe Solar Cell Performance," B.E. Proc. 22nd IEEE PVSC, 967

39. D. K. Schroder, 2005. "Semiconductor Material and Device characterization" 3rd Ed. Wiley Inter-Science.

40. S. M. Sze, 1981. Physics of Semiconductor Devices, 2nd Ed. John Wiley and Sons, NY.

41. S. S. Hegedus, W. N. Shafarman, 2004. "Thin Film Solar Cells: Device Measurements and Analysis, Prog. Photovolt: Res. Appl. 12: p 155-176

42. J.D. Cohen, J. T. Heath and W. N. Shafarman, 2003. Distinguishing metastable changes in bulk CIGS defect densities from interface effects, Thin Solid Films 431 – 432 (2003) 426 – 430.

43. J. T. Heath, J.D. Cohen and W. N. Shafarman, 2004. "Bulk and metastable defects in $CuIn_{1-x}Ga_xSe_2$ thin films using drive-level capacitance profiling", J. Appl. Phys. Vol. 95, No. 3, 1000- 1010

44. Walter, T. and Herberholz, R. and Müller, C. and Schock, H. W., 1996. "Determination of defect distributions from admittance measurements and application to Cu(In,Ga)Se2 based heterojunctions". J. Appl. Phys., 80, 4411-4420

45. Herberholz, R. M. Igalson, and Schock, H. W., 1996. "Distinction between bulk and interface states in CuInSe2/CdS/ZnO by space charge spectroscopy". J. Appl. Phys., 83, 318.

46. Jian V. Li, and Levi, Dean H., 2011. “Determining the defect density of states by temperature derivative admittance spectroscopy” , J. Appl. Phys., 109, 083701

47. J. H. Scofield, 1994. “Effect of series resistance and inductance on solar cell admittance measurements” Sol. Ener. Mat. And Sol. Cells 37, 217 - 233

48. Eisenbarth, Tobias and Caballero, Raquel and Nichterwitz, Melanie and Kaufmann, Christian A. and Schock, Hans-Werner and Unold, Thomas, 2011. “Characterization of metastabilities in Cu(In,Ga)Se2 thin-film solar cells by capacitance and current-voltage spectroscopy”, J. Appl. Phys., 110, 094506

49. Labsphere UV-VIS User Guide

50. J. Hilfiker, R. Synowicki, H.G. Tompkins. “Spectroscopic Ellipsometry Methods for Thin Absorbing Coatings”, SVC 51st Annual Tech. Conf. Proceedings, (2008) 511-516.

51. J. A. Woollam, B. Johs, C. Herzinger, J. Hilfiker, R. Synowicki, and C. Bungay. “Overview of Variable Angle Spectroscopic Ellipsometry (VASE), Part I: Basic Theory and Typical Applications”, *SPIE Proceedings*, CR72, (1999) 3-28.

52. Mutitu, J.G.; Obahiagbon, U.; Shouyuan Shi; Shafarman, W.; Prather, D.W., 2014. "Light Trapping in Thin-Film Cu(InGa)Se 2 Solar Cells," Photovoltaics, IEEE Journal of , vol.4, no.3, pp.948,953

53. Demtsu, S.H.; Sites, J.R., 2005 "Quantification of losses in thin-film CdS/CdTe solar cells," Photovoltaic Specialists Conference, 2005. Conference Record of the Thirty-first IEEE , vol., no., pp.347,350

54. J. R. Sites, 2003. “Quantification of losses in thin-film polycrystalline solar cells”, Sol. Ener. Mat. and Sol. Cells, 243 – 251

55. M. Gloeckler and J. R. Sites, 2004. “Efficiency Limitations for Wide-bandgap Chalcopyrite Solar Cells”. Thin Solid Films 480 - 481 (2005) 241 – 245

56. Marc Burgelman*, Johan Verschraegen, Stefaan Degrave and Peter Nollet, 2004. “Modeling thin-film PV devices”, Prog. in Photovolt: Res. and Appl. Vol. 12, Iss. 2-3, pp 143 – 153.

57. M. Burgelman, P. Nollet and S. Degrave, 2000. "Modelling polycrystalline semiconductor solar cells", Thin Solid Films, 361-362, 527-532.

58. Peter T. Erslev, JinWoo Lee, Gregory M. Hanket, William N. Shafarman, J. David Cohen, 2011. "The electronic structure of $Cu(In_{1-x}Ga_x)Se_2$ alloyed with silver", Thin Solid Films, Vol. 519, Iss. 21, 31, pp. 7296-7299.

59. JinWoo Lee, J. David Cohen, William N. Shafarman, 2005. "The determination of carrier mobilities in CIGS photovoltaic devices using high-frequency admittance measurements". Thin Solid Films, Vol. 480–481, pp. 336-340.

60. W. K. Metzger and M. Gloeckler, "The impact of charged grain boundaries on thin-film solar cells and characterization" J. Appl. Phys. 98 (2005) 063701.

61. M. Gloeckler, Dissertation, Device Physics of Cu(In, Ga)Se2 Thin-Film Solar Cells, (2005)

62. Marc Burgelman □, Koen Decock, Samira Khelifi, Aimi Abass, 2013. "Advanced electrical simulation of thin film solar cells", Thin Solid Films 535, 296 - 301

63. Green, Martin A., Emery Keith, Hishikawa Yoshihiro, Warta Wilhelm, Dunlop Ewan D., 2014. Solar cell efficiency tables (version 43) Prog. Photovolt: Res. Appl.Vol. 21, Issu. 5, pp. 827 - 837.

64. S. Siebentritt, L. Gutay, D. Regesch, Y. Aida, V. Depredurand, 2013. "Why we make CIGS solar cells non-stoichiometric". Sol. Energy Mat. And Sol. Cells 119, 18-25.

65. J. E. Phillips and W. N. Shafarman, 1999. "Analysis of CIGS solar cells: why performance decreases with increasing Ga content". AIP Conf. Proc. 462, 120

66. E.Centurioni, 2005. "Generalized matrix method for calculation of internal light energy flux in mixed coherent and incoherent multilayers", Applied Optics, Vol. 44, No. 35, pp 7532-7539

67. A. C. Marsh and J. C. Inkson, 1986. "Scattering matrix theory of transport in heterostructures", Semicond. Sci. Technol. 1, 285 – 290.

68. Kkotnim Lee, Eun-A Ok, Jong-Keuk Park, Won Mok Kim, Young-Joon Baik, Donghwan Kim, and Jeung-hyun Jeong, 2014 The Impact Of Oxygen Incorporation During Intrinsic ZnO Sputtering on The Performance of Cu(in,ga)se2 Thin Film Solar Cells, Appl. Phys. Letters 105, 083906

69. A. M. Gabora, J. R. Tuttlea, M. H. Bodea, A. Franza, A. L. Tennanta, M. A. Contrerasa, R. Noufia, D. G. Jensenb, and A. M. Hermannc. 1996. " Band-gap engineering in Cu(In,Ga) Se2 thin films grown from (In,Ga)2Se3 precursors". Sol. Energy Mater. Sol. Cells 247 - 260

70. P. D. Paulson, R.W. Birkmire, W. N. Shafarman, 2003 “Optical Characterization of CuIn1-xGax Se2 Thin Films by Spectroscopic Ellipsometry”, J. Appl. Phys. vol. 94, 879-888

71. P. Jackson et al, 2007. “High Quality Baseline for High Efficiency, CIGS Solar Cells”. Prog. Photovolt. Res. Appl.; 15: 507-519

72. Repins et al, 2008. “19.9%-efficient ZnO/CdS/CIGS Solar Cell with 81.2% Fill Factor”. Prog. Photovolt. Res. Appl.; 16:235-239

73. Streetman, B., Banerjee, 1999. Solid State Electronic Devices, 5th edition, Prentice Hall