OPTIMIZING FABRICATION TECHNIQUES OF MATERIALS AND DEVICES FOR INTEGRATED NANOPHOTONICS

by

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ABSTRACT

Photonics is a branch of science which deals with the manipulation of light (“photons”) and has been growing exponentially in the last few decades due to the increased demands for faster data transfer, larger bandwidth, lower loss, lesser power requirement etc. To make these photonic devices we need to fabricate different active and passive device components. In this thesis, we have described the fabrication methodology and optimization techniques for such different photonic components. The thesis also discussed about different materials which find application in photonic devices.

We discuss the importance of Silicon photonics and discuss the fabrication of different components namely waveguides, diffraction grating couplers, micro-ring resonators and photonic crystal waveguides. We explain in detail the process flow of fabrication of these components and the various challenges involved in each case. We also explain the methodology to overcome these problems and discuss optimization methods to improve the device quality. We characterize the quality of these components using loss analysis and performance measurements. We have explored the possibility of using amorphous silicon instead of crystalline silicon in photonics and tried understanding the limitations and possible ways to overcome them. We have also extended our study to bulk chalcogenides namely germanium antimony telluride (GST) by physical vapor deposition and indium selenide by exfoliation methods as materials having different applications in photonic industry. Beyond silicon we have extended our work to explore possibilities of two dimensional (2D) materials like graphene and organic materials in photonics. Some advanced applications are highlighted, the details of which will be reported in our future work.

Chapter 1

INTRODUCTION

1.1 Background

Silicon is one of the most abundant element on earth and has found application in almost every single gadget that we use today due to its semiconductor properties. We owe our current technological advancement due to the mature microelectronics industry which flourished around silicon to manufacture semiconductor devices which can modulate electrons. Silicon has dominated the electronic industry for decades and is one of the most well-studied material for fabricating electronic components and devices. With the increase in computing advancement requiring higher data bandwidth, lesser power dissipation, high volume manufacturing and lesser cost; the electronic transistors impeded the growth in high speed and high-performance requirement needed for future computing platforms. Thus there was a necessity to have a paradigm shift from using electrons to photons for communication and interconnects in computing. Thus to keep up with Moore's law, where the number of transistors in a single die for a chip doubles ever two years it was important to shift from "electron" to "photons" that is where photonics – the science of modulation and manipulation of light (photons) comes into picture. Presently we are seeing a convergence of electronics and photonics to obtain high-performance computing systems. Silicon is once again considered a promising candidate for photonics due to multiple reasons. Firstly, silicon can be easily integrated to the current CMOS technology electronics and the fabrication knowledge of decades in the microelectronic industry can be easily transferred to photonic industry thereby making the transition easier as compared to a new material. Secondly, silicon has a bandgap of

1.1 eV which means that it is transparent to a wavelength above 1.13 μm. The near-IR transparency combined with the high refractive index contrast between silicon (n of Si = 3.45) - silicon dioxide (n of SiO_2 = 1.45) is advantageous to manufacture waveguides for telecommunication applications which work at 1.3 μm and 1.5 μm. Therefore silicon can be used for fabricating low propagation loss waveguides thereby enabling lower power dissipation and lesser energy consumption per bit. The state of the art production line capabilities to make nano-structured devices combined with lower cost and its compatibility with silicon electronics makes it a material of choice for the photonics industry. There has been rapid progress in the integrated silicon photonics field resulting in high data throughput, lower packaging cost, electronic-photonic integration on chip and development of processes which doesn't damage the electronic counterpart. In this thesis, we have explored the fabrication process of different passive and active devices on silicon on insulator (SOI) platform and the challenges associated with it. As a new research group at the University of Delaware, we have exploited the facilities at the University of Delaware Nanofabrication Facility (UDNF) to fabricate devices on SOI and other platforms. We have tried understanding the problems associated with the fabrication methods and optimize the process to make functional devices. We have also explored materials other than silicon to find applications in nanophotonics and studied their material properties and results on prototype devices. The different techniques in which we can grow or transfer them on photonic structures have been explained. We have also discussed applications of the active and passive devices fabricated, the results of which will be shown in our future work.

1.2 Thesis Outline

In chapter 2, we have discussed about the generic fabrication process for the photonic devices on SOI platform. The process flow has been explained in detail highlighting the challenges and the solutions to overcome them in the fabrication methodology. Different active and passive devices are discussed and the process-specific issues are examined. The applications and the results of these devices are also explored. Chapter 3 discusses about materials beyond silicon which can find application in silicon photonics. We have explored amorphous silicon (a-Si:H), bulk chalcogenide materials, 2D materials and even organic materials which can find applications in future nanophotonic devices. The different fabrication methods, transfer techniques and properties are elucidated in this chapter. Chapter 4 summarizes the results and conclusion from our work and outlines future goals.

Chapter 2

FABRICATION OF DEVICES FOR NANOPHOTONICS

2.1 Fabrication Process:

In this section, we have discussed the generic fabrication process flow for all the active and passive photonic devices listed. Process steps which are specific to a certain type of device have been discussed in the respective section of that device. Similarly, the challenges and solutions to technical problems in a specific device have also been addressed in the relevant section. For fabricating the photonic structures we have used 220 nm silicon with 2 μm buried oxide as well as 250 nm silicon with 3 μm buried oxide SOI wafers having a base wafer thickness of 675 μm. The standard fabrication steps for the different devices are as mentioned below:

- ***Organic Clean***

Before the start of the fabrication process, it is important that the chip is free of any contaminants or residue. An effective way to clean the SOI chip or a-Si:H on glass is to subject it to solvent cleaning. The widely used solvent cleaning method in laboratories is Acetone-Isopropyl Alcohol-Deionized water (DI) rinsing method. Acetone [$(CH_3)_2$-CO] is an organic solvent which is capable of dissolving most of the organic residues. Therefore, the 1st step is to sonicate the chips for 5 minutes in Acetone. Since acetone leaves a film of organic residue after it quickly dries from the surface, it is important to dissolve the acetone before it dries. Hence we immediately transfer the substrates to Iso-propyl alcohol (IPA) before the acetone dries. IPA [CH_3-CH-OH-CH_3] helps to rinse the residual acetone from the surface. It is hygroscopic and displaces water hence it leaves the surface of the substrate dehydrated without any

spots or film residue. Thus the 2nd step is to sonicate the substrate for 5 minutes in IPA. Care should be taken to not let the surface of the substrates to dry since this will leave any organic residue which can hinder the fabrication process at a later stage. After IPA rinsing the substrate is immediately rinsed in DI water followed by blow drying with Nitrogen to clean the surface of any water residue.

- ***Plasma Cleaning***

Plasma cleaning is a 2nd cleaning step usually done after the organic clean to further remove any organic contaminant from the surface. Unlike the wet method used in the previous step, it is a dry method involving gaseous plasma as the cleansing agent. Also, the previous mechanism involves physical cleaning whereas this method is a chemical cleaning process. We use gaseous plasma of oxygen to strip any organic matter at the surface. The oxygen plasma produces different metastable ions and radicals like O^-, O^{2-}, O^+, O^{2+} etc which reacts with the organic matter and forms carbon residue at the surface called 'ash'. Hence the process is also known as 'Plasma Ashing'. The carbon residue further reacts with the free radicals to form volatile byproducts like carbon dioxide and water vapor which are pumped out using vacuum pumps. We use a 2 step ashing process, the first step at 400W for 50 seconds followed by 800W for 600 seconds at a pressure of 1.5 Torr with an oxygen flow of 1000 sccm. We have used a 13.56MHz RF (Allwin 21 Corp. AW-B3000) barrel plasma asher with Branson PC controller for this step.

- ***Substrate Priming***

For fabrication of the photonic components, one of the major problems could be the adhesion issue of the resist. Adhesion of the resist is of prime importance since poorly adhered resist can cause breakage of the waveguide patterns as well as improper development of the patterns. Figure 2.1 shows the breakage in waveguides due to poor adhesion. Therefore, there are 2 methodologies which we have used in our fabrication process to minimize this issue, the details of which are mentioned below.

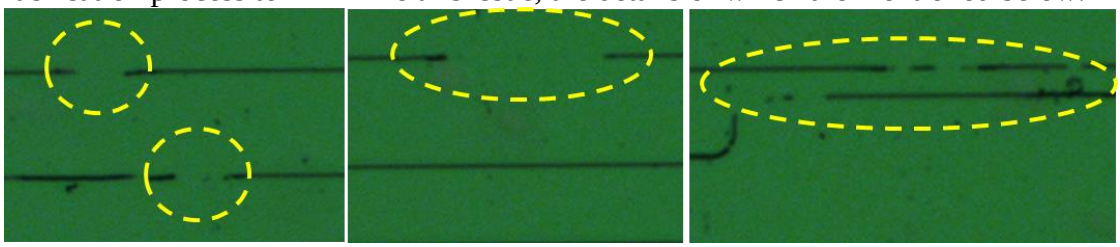

Figure 2.1 – Optical microscope image showing breakage in waveguide due to adhesion issue

One of the techniques that we have used to remove adhesion issue is to treat the substrate with HMDS (hexamethyldisilazane) at a pressure of 1000 mTorr and temperature of 150 °C in a convection oven, which helps to repel any water on the surface of the substrate. In our process, we have used HMDS in vapor phase instead of the liquid phase to get uniform coverage and complete dehydration of the surface. The complete dehydration of the surface is made sure with the high temperature combined with the pump-purge cycle with nitrogen which removes any possible moisture. Since this step is formed after the plasma asher, usually a thin oxide layer exists after the ashing in oxygen which is advantageous for the growth of HMDS due to the fact that HMDS has better adhesion to oxide as compared to silicon. Thus a monolayer of HMDS grows on the substrate making the surface hydrophobic. This step is important

because HMDS avoids any moisture getting trapped between the resist and the substrate which can lead to lift-off of the resist during development, resulting in breakage as shown in Figure 2.1 above. Thus as against the belief, HMDS does not improve the adhesion of the surface rather removes any moisture content which can interfere with pattern development. Hence it is important that the process is optimized to not form multilayers of HMDS which can make the surface too hydrophobic preventing the wetting of the surface with resist during spin coating.

Another method to improve the adhesion is to use adhesion promoters spin-coated on the substrate. The adhesion promoter usually contains organosilanes which contain an inorganic reactive end at one side of the molecule and inorganic reactive component at the other side of the molecule. The inorganic reactive end binds with silicon whereas the organic reactive end binds to the resins in the resist, thereby improving the wettability of the resist. In our experiments, we have treated the substrates with adhesion promoter AR-300-80 by Allresist. It is spin coated at 4000 rpm for 1 minute to give a thickness of ~15 nm then baked at 180 °C for 2 minutes. We have found that using Adhesion promoter is a better alternative to HMDS since it gives lesser breakage and is cheaper than HMDS making it economically viable.

- ***Spin Coating of Resist***

In order to write the photonic structures pattern on the substrate, it has to be spin-coated with E-beam resist. In our process, we have used both positive and negative resist. A Brewer science spin-coater and bake plate combination is used for this step. For negative resist, AR-N-7520-18 by Allresist GmbH is used due to its high

resolution (<30nm), high contrast (>5) and plasma etching stability. It consists of resins like phenol formaldehyde, cross-linking compounds like Propylene glycol methyl ether acetate (PGMEA) in solvent. The resist is dispensed using a pipette onto the wafer held by a vacuum chuck and it is rotated at a speed of 4000 rpm for ~ 60 seconds where the coat of ~400 nm is applied. The negative resist gave particulate residue due to which some of the designs were fabricated using a positive resist pattern. From Figure 2.1 we can see that for the same pattern by the positive and negative resist, we can see particulate residue for the negative resist. Therefore, for processes which are sensitive to such particulate residue, it would be more advisable to switch to the positive pattern. For such process, we spin-coated the sample with positive e-beam resist AR-P-CSAR 6200 (.09) by Allresist. It has higher contrast (>15) and resolution of upto 10 nm. It is spin coated at 4000 rpm for 1 minute giving a thickness of ~180 nm.

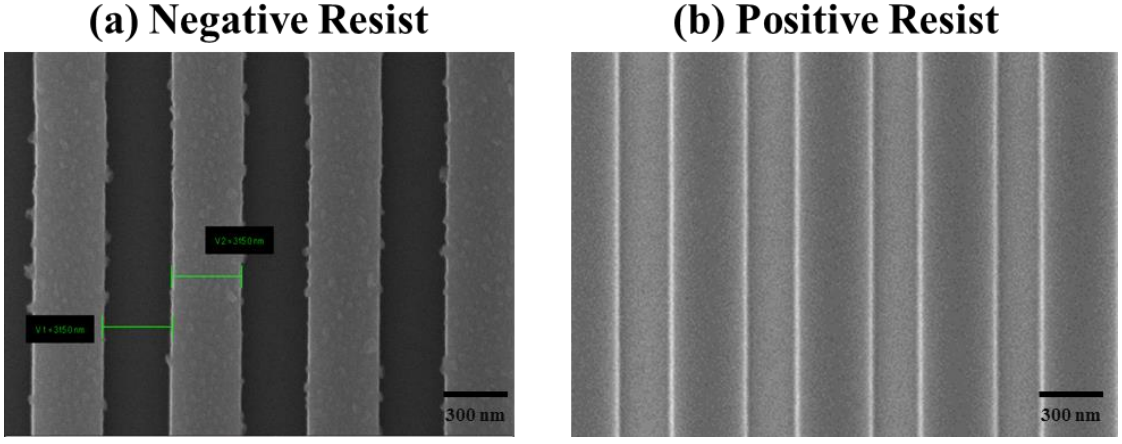

Figure 2.2 – Scanning Electron Microscope (SEM) image of (a) Negative resist AR-N-7520-18 (b) Positive Resist AR-P-CSAR 6200 (.09) pattern developed after electron beam lithography. The particulate residue can be seen on the negative resist which is absent on the positive resist

Thickness (t) of the coat is related to the angular velocity (ω) as follows [1]:

$$t\alpha \frac{1}{\sqrt{\omega}}$$

The spinning of the resist results in gradient shearing stress across the fluid due to the centrifugal force giving a uniform film of resist having a fixed thickness. The spin curve shows the decline in the thickness of the resist as the spin speed increases and it only additionally depends on the viscosity of the resist. It is important to not have any particles on the substrate during this step since the particles result in comet trails which affect the writing of the pattern during E-beam lithography. The edge of the sample has thicker resist called as edge bead which limits the area in which we can do lithography. Usually, this region is not considered for lithography due to the non-uniformity in the resist thickness.

After spinning the resist, the next step is 'soft baking' the resist which helps to evaporate the solvents in the resist. Solvents in the resist help for spin coating the resist as well as dispensing it, however, it is important to remove any trace of solvent in the film before lithography since the solvent can deform or enlarge the exposed area resulting in poor pattern transfer. For the negative resist AR-N-7520-18 the bake temperature is 85 °C for 1 minute. Whereas the positive resist is baked in hot plate at 170 °C for 5 minutes.

- ***E-Beam Lithography***

Since the photonic structures need high precision and have feature sizes of the order of nanometers we use Electron-beam lithography (EBL) to write the patterns on

the resist. EBL uses an electron beam where the wavelength (λ) of the electron depends on its Energy (E) by the de Broglie equation where

$$\lambda = \frac{h}{\sqrt{2mE}}$$

In this equation, h is Planck's constant and m is the mass of the electron. Thus EBL produces electrons having wavelength of the range of picometers enabling writing nanometric features with high precision. EBL is a direct write tool which does not involve any photomask. The stitching errors in the field boundaries have been compensated by using multipass writing. The design files were made using Clewin software and the .gds files were used to write the pattern on to the substrates. For the negative resist, we use an exposure dose of 500 μC/cm².

- ***Development Process***

After selectively exposing the resist to an electron beam as explained above, its chemical structure changes. It now undergoes development process. Development selectively removes exposed or unexposed photoresist layer, depending on whether it underwent positive or negative pattern transfer. This selective removal is based on the fact that the exposed and the unexposed regions have a difference in solubility over several orders of magnitude. This step is very critical and as we will see in the text ahead underdevelopment or overdevelopment can adversely affect the feature size and device performance. For the negative resist, we have used developer by Allresist, AR-300-47 (4:1) H_2O for 90 seconds followed by DI water rinse for 60 seconds and N_2 drying the sample. Most of these developer solutions are a mixture of metal hydroxides with surfactants, solvents and buffers to maintain pH of the solution. The developer solution we have used is metal ion free which uses Tetramethylammonium

hydroxide (TMAH), an ammonium quaternary hydroxide instead of metal hydroxide to avoid metal contamination.

- ***Dry Etching/ Plasma Etching***

Plasma etching is an important method which uses neutral free radicals and ion in plasma to etch the region unprotected by the photoresist. The difference between a plasma etching and plasma deposition technique is that plasma etching produces volatile byproducts which get pumped out, unlike plasma deposition which produces nonvolatile byproducts. The cumulative effect is the metastable species react with the substrate to etch it resulting in negative film growth rate. When a plasma is generated only a small fraction of the feed gas is dissociated into neutral free radicals and charged ion species. Out of this the fraction of free radicals is more than the ion species and is mostly responsible for the etching. The etching process involves different chemical processes like the dissociation of neutral and charged species, attachment and detachment of electrons to neutral as well as charged particles, recombination of charged and free radicals, sputtering, adsorption, desorption etc. making the overall process complex to quantitatively understand. Hence usually a more qualitative approach is provided. The plasma etching is anisotropic since the reactivity is more horizontal than vertical (since the radicals impinge more on the horizontal surface than the vertical surface) which plays a pivotal role in define the sidewall roughness which is critical for photonic application. For our experiments, we have used inductively coupled plasma (ICP) etching process in which a time-varying magnetic field excites and sustains the plasma [2]. Since there is no net electric field the ion bombardment damage to the substrate is minimized. An additional DC bias can

control the ion bombardment, thus we can have a combination of chemical as well as mechanical sputtering etching.

In our experiments, we have used ICP-RIE (Inductively coupled plasma – reactive ion etching) tool by Plasma-Therm to etch the pattern. The tool has back-side helium cooling for constant substrate temperature. We have used Sulphur hexafluoride (SF_6) and octafluorocyclobutane (C_4F_8) mixed plasma to etch the silicon. The SF_6 gas forms radicals which react with silicon to form SiF_4 which is a gas at room temperature and gets pumped out resulting in the etching of silicon. This process involves multiple reaction steps involving free F radicals and neutral SF_x species where the reaction with the least activation energy dominates the process. Purely SF_6 plasma etches silicon by chemical etching rather than mechanical etching. Hence the etching is more isotropic. The by-product Sulphur does not form a passivation layer and hence the surface has higher surface roughness. Due to this reason, SF_6 is usually combined with carbon tetrafluoride (CF_4) or octafluorocyclobutane (C_4F_8). The additional CF radicals in the plasma form long chain fluoropolymers which are non-volatile and inert. This layer passivates the surface and prevents further etching of the surface from the SF_x radicals. The DC bias voltage causes the ion bombardment which removes these non-volatile films by sputtering action. Thus fresh Si surface is available for reaction. This process of deposition and etching is advantageous to reduce the surface roughness of the sidewalls and edges which is especially critical in photonic structures where surface roughness can introduce losses in waveguides. Thus a mixed plasma results in a directed and anisotropic etching making the etching highly selective.

In order to get vertical sidewall and prevent over-etching of the features, it is important to know the etch rate of silicon (both crystalline and amorphous) as well as know the resist to silicon selectivity. This can be obtained by the methodology shown in Figure 2.3. We first measure the thickness of the features of the resist by using a Dektak profilometer. For example for the negative resist AR-N-7520-18 mentioned in the previous section, for the spin speed of 4000 rpm, we get a thickness of 400 nm. As shown in Figure 2.3 on SOI we get a thickness of 388 nm (average of 10 measurements) and for a-Si, we get a thickness of 342 nm (average of 10 measurements). We then etch the developed sample for a fixed time 't' which will etch a certain thickness of the resist and the silicon substrate. Let's say X nm and X' nm of resist remains in SOI and a-Si substrate respectively and we measure the thickness of the features after etching. We find that for SOI the thickness after etching is 514 nm which is a combination of X nm of resist + 250 nm of silicon + Y nm of the oxide (assuming the sample might have over-etched during time t). Similarly, for a-Si after etching, the thickness is 411 nm, which is a combination of X' nm of resist + 250 nm of a-Si. We then plasma ashed the samples to completely strip the resist and re-measure the thickness of the features averaged 10 times. We found that after plasma ashing, the height of the features is 255 nm for SOI and 117 nm for a-Si. This meant the SOI was slightly over-etched by 5 nm and the thickness of the remaining resist after ICP etching is X = 259 nm. The etch rate of crystalline silicon is 7.35 nm/sec and the c-Si: Resist selectivity is 2:1. On the other hand, for a-Si pattern the features are under-etched. The thickness of the remaining resist after ICP etching is X = 294 nm. Thus the etch rate of a-Si is 6.5 nm/ sec and the a-Si: Resist selectivity is 2.8:1.

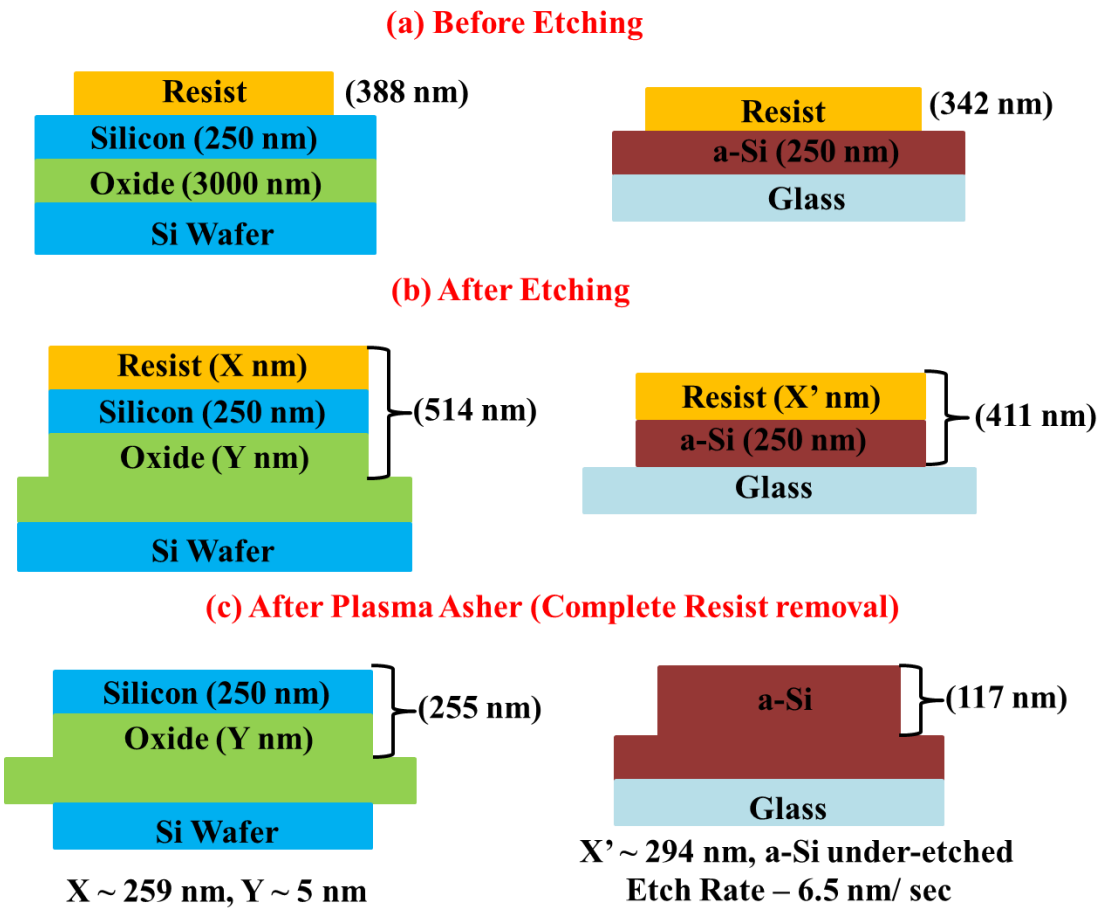

Figure 2.3 – Methodology to find the etch rate as well as resist to substrate etch selectivity for crystalline as well as amorphous silicon.

For etching 250 nm silicon on SOI wafer, the etch rate we have used is 425 nm/min (7.08 nm/sec) and it takes ~35 seconds to etch the silicon pattern. Based on the resist we use the selectivity of Si: Resist is between 2:1 to 3:1 in all our experiments. Usually, the PR residue after etching is removed either by plasma ashing or NMP (N Methyl Pyrrolidone or 1-Methyl-2-pyrrolidone) is used for stripping the resist.

2.2 Waveguides

Waveguides are the basic building block of photonic technology which enables light propagation. For integrating into photonic circuits it is important for waveguides to have lower propagation loss. Therefore fabrication of waveguides needs some serious constraints which have to be implemented for it to be used effectively in an integrated photonic circuit. The waveguide fabrication should not involve any high-temperature process which can damage the combining electronics and the fabrication techniques should complement the currently used technology in microelectronics to make it industrially viable. Therefore, silicon in a good contender to be a waveguide material due to its mature processing technology in microelectronics. In this section, we have discussed the challenges and process optimizations to fabricate waveguides on silicon i.e. both crystalline and amorphous silicon. Silicon forms the core material in the waveguide for light propagation usually having a silica cladding layer. Silicon having high refractive index helps to have lower bending radius and makes the circuit ultra-compact helping to reduce packaging cost. There are different types of waveguides like strip, rib and buried waveguides for different applications, however, we have used strip waveguide for most of our study and reference to any waveguide would mean strip waveguide unless specified otherwise.

2.2.1 Waveguides Fabrication

One of the primary pre-requisite for waveguide fabrication is the absence of any form of contaminants on the surface of the substrate which can act as light scatterer and thereby introducing loss. Another requirement is the sidewall roughness which has to be minimized to decrease scattering losses in the waveguide by having vertical sidewalls by anisotropic etching. In this section, we have elaborated the

methodology to obtain these requirements by optimizing the process conditions. After following the standard fabrication method as described in section 2.1 we observed multiple bottlenecks which affected the quality of the photonic structures made. Some of the major problems faced and their solutions are elucidated in this section.

One of the observations was that there were particles contaminants in the final device fabricated as shown in Figure 2.4 leading to either increased propagation loss or waveguide breakage.

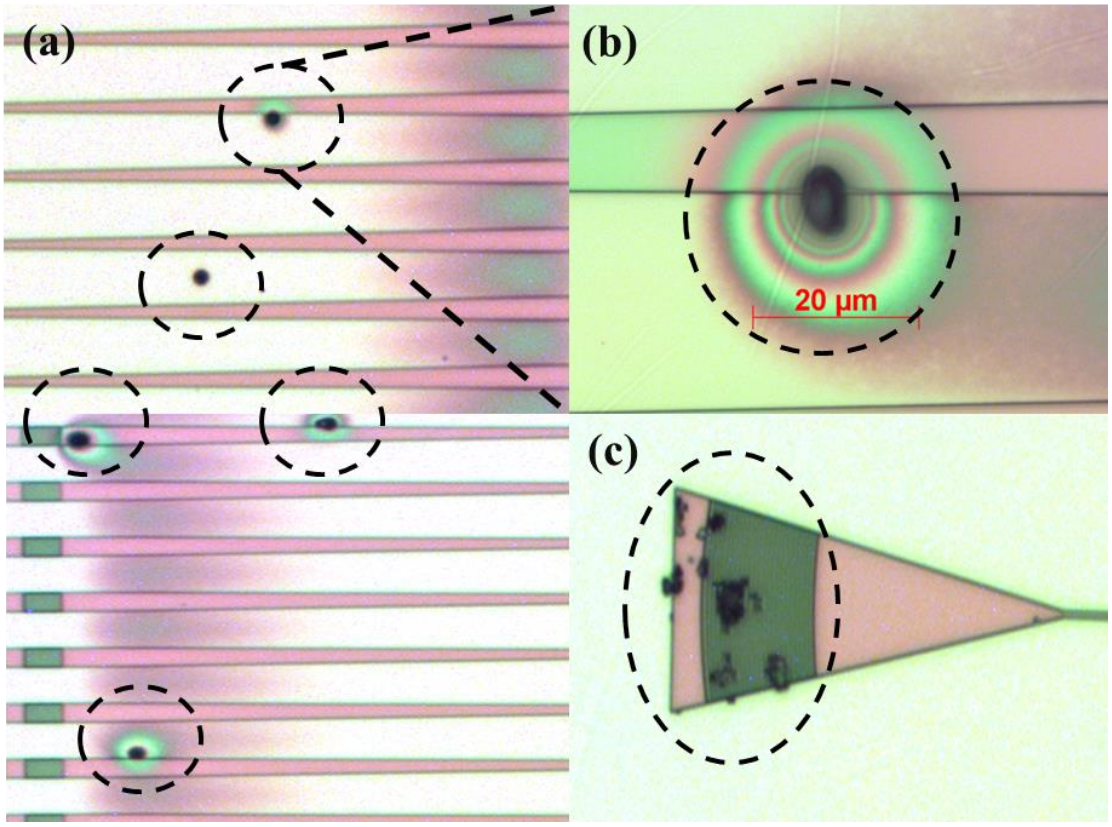

Figure 2.4 – Optical microscopy of (a) Particles on the surface of the patterned waveguide surface (b) Enlarged image of the particle on the pattern after development (c) Debris found on the coupler of the waveguide

In order to overcome this problem, it was important to understand the source of this contamination. Our first approach was to investigate the surface before spin coating the resist and observation of the surface under dark-field microscopy which revealed that there was particulate residue on the surface that were invisible in light-field microscopy resulting in particles causing waveguide breakage during development/ etching stage. This problem was resolved by using an additional pre-clean step. For this pre-cleaning, we have used Nanostrip, which is a mixture of sulfuric acid (H_2SO_4), hydrogen peroxide (H_2O_2) and a stabilizer working much like a Piranha solution. We use Nanostrip solution at 80 °C to clean the substrate followed by rinsing the samples in DI water. We then post-bake the samples in a hot plate at 170 °C for 5 minutes. This step is critical in removing any additional organic contaminant from the surface as well as any metal residues on the surface. In the absence of the above cleaning method, we find particulates on the surface of the chip as shown in Figure 2.5 which can affect the transfer of the design. In Figure 2.5 which is a dark field optical micrograph of the surface before and after Nanostrip cleaning clearly shows the reduction in the particles on the surface of the wafer. It is advisable to take dark field images before and after every step of cleaning to verify that the contaminants are completely removed, either during optimizing a new process or while using a new batch of SOI wafer. Incase if there is a need to save time, we should at least observe the dark field image after the entire cleaning process to verify the chip is suitable for EBL. An additional process done to reduce particulate contaminant is to filter the resist before spin coating especially for negative resist as shown in Figure 2.2.

(a) Before Cleaning **(b) After Cleaning**

Figure 2.5 – Dark Field imaging of the surface after plasma ashing (a) Before and (b) After Nanostrip cleaning.

Another problem was the vertical sidewall in the waveguide which can introduce losses. For the waveguide to have minimal propagation loss due to scattering at the edges, it is imperative to get straight sidewalls. For this, we optimized our dry etching recipe to make it anisotropic by using a combination of SF_6 and C_4F_8 so that the resultant etching is a combination of chemical as well as mechanical etch. Argon (Ar) was used to dilute the reactive gases and also assist mechanical sputtering. Figure 2.6 shows a strip waveguide adjacent to a micro-ring resonator. The cross-sectional image of the waveguide shows that we have straight sidewalls reducing the losses in the waveguide.

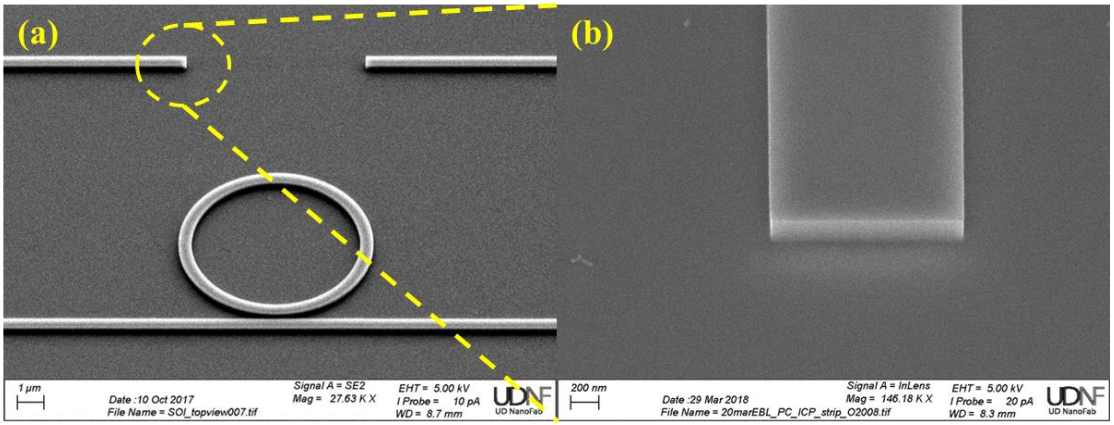

Figure 2.6 – (a) Tilted angle SEM of strip waveguide running alongside of a microring resonator (b) Enlarged cross sectional SEM of the same waveguide showing smooth sidewalls after ICP RIE etching

Therefore by introducing a pre-clean step in the form of Nanostrip and optimizing the dry etch recipe we reduced the problem of particulates on the surface and side-wall roughness. In order to further eliminate any particles coming from the negative resist we also introduced a positive resist process. For the positive pattern transfer, we first spin-coated with positive resist AR-P-CSAR 6200 (.09) at 4000 rpm for 1 minute spin to give an approximate thickness of 180 nm. It was then baked in a hot plate at 170 °C for 5 minutes. After EBL at a base dose of 200 $\mu m/cm^2$ we developed it using AR-600-546 for 1 minute followed by rinsing with IPA for 30 seconds. The etching process remains the same as the previous steps mentioned in section 2.1. Figure 6 shows the waveguide fabricated. The dark field image in Figure 2.6.a shows no breakage or particles in the final strip waveguide, similarly, the SEM micrograph verifies the thickness and the edge roughness as shown in Figure 2.6.b. The characterization of these waveguides are shown in section 2.2.2.

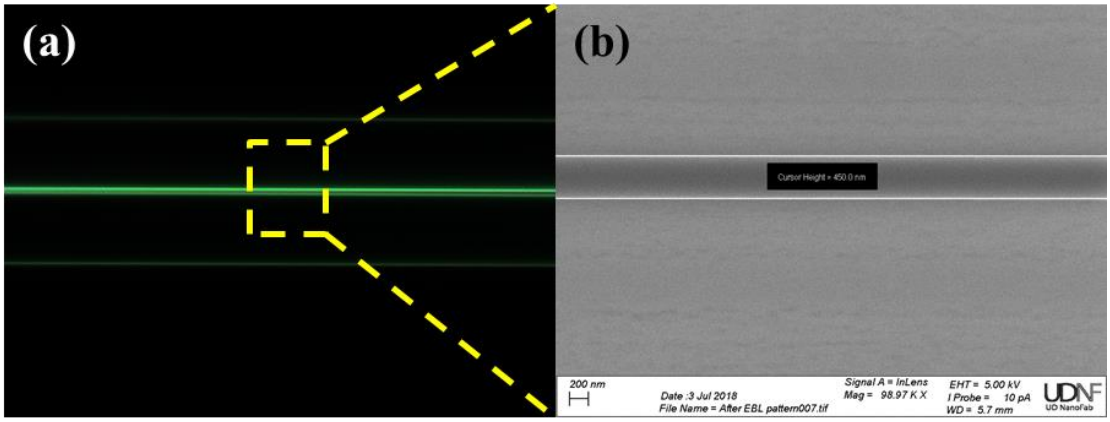

Figure 2.7 (a) Dark Field microscopy of strip showing no defects or breakage (b) SEM top view of the same waveguide measuring 450 nm with smooth edges

2.2.2 Loss in Waveguides

This section talks in detail about the characterization of the waveguide fabricated and a good method to understand the quality of these waveguides is by measuring the losses in them. The intrinsic loss in silicon is almost negligible since the bandgap of silicon is 1.1 eV, it is completely transparent in the telecommunication wavelength range of 1300-1550 nm, where we want it to operate. Thus at this wavelength range, the propagation loss is dependent on the scattering loss due to the surface roughness of the waveguide. It is for this reason that in the previous section we optimized the etch recipe to get smooth edges. It is important to note that the maximum scattering loss (α_{max}) is directly proportional to square of the root mean square (r.m.s) roughness of the surface of the waveguide (σ) i.e. $\alpha_{max} = K. \sigma^2$ where K depends on waveguide geometry and effective refractive index as given by Payne et.al.[3]. For practical fabrication purposes, the surface roughness should be less than 1 nm to obtain loss less than a few dB/cm. For measuring the propagation loss we have taken the structure shown in Figure 2.8.a having waveguides of different width

(400 nm and 500 nm) and their loss for different length is measured. The setup to measure the loss is shown in Figure 2.8.b and 2.8.c. The design has a different length of waveguide and the loss at different length helps us to plot the graph of loss versus length. The slope of this curve helps to determine the loss per cm in the waveguide as well as the loss per facet. Table 2.1 shows the data of the loss in the waveguide for different length when Width (W) = 400 nm and W = 500 nm. The plot of the Loss Vs Length for the two widths along with the curve fitting parameters is shown in Figure 2.9.a and 2.9.b. We find that for W = 400 nm we have a loss of -12 dB/cm with each facet having a grating coupling loss of -14 dB. Similarly, for W = 500 nm, the loss is -6.04 dB/cm with each facet having a grating coupling loss of -18.3 dB. All the propagation loss measurement is done at 1550 nm wavelength. For the waveguides fabricated using positive pattern transfer, we find that the propagation loss is -6.56 dB/cm and grating coupling loss per facet is -13.5 dB.

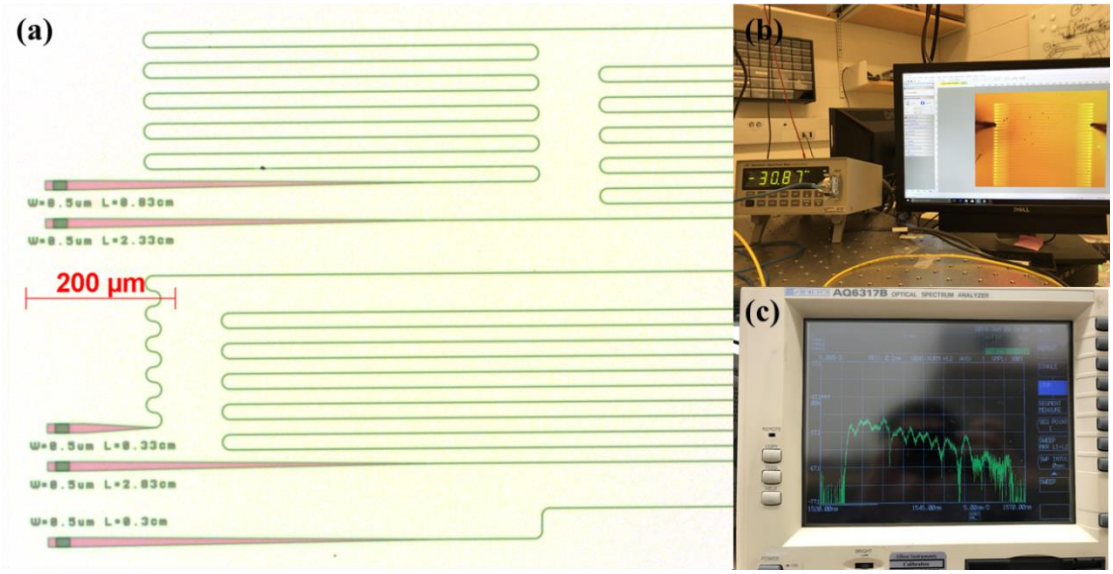

Figure 2.8 (a) Layout to measure propagation loss in strip waveguide having different width (b) setup to measure propagation loss (c) Spectrum analyzer

(Image Credit: Dun Mao)

Table 2.1 – Propagation Loss measured in waveguide having different width

Width = 500 nm		Width = 400 nm	
Length (cm)	**Loss (dB)**	**Length (cm)**	**Loss (dB)**
0.3	-38.76	x	X
0.33	-33.02	0.33	-34.35
0.83	-41.17	0.83	-38
1.33	-44.73	1.33	-43.81
1.83	-47.56	1.83	-48.87
2.33	-53.83	2.33	-60.01
2.83	-58.83	2.83	-62.47

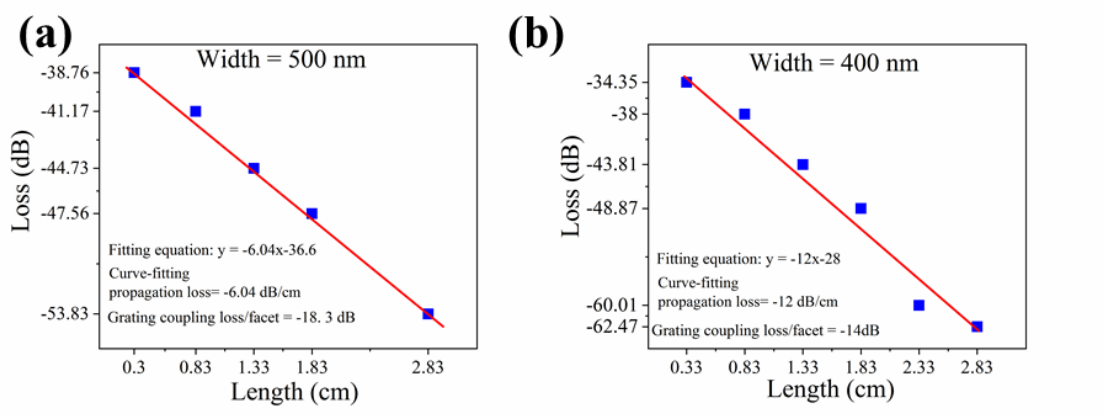

Figure 2.9 – Linear curve fitting of propagation loss at different length for (a) W = 500 nm and (b) W = 400 nm

(Credit: Dun Mao)

Another loss which is of importance in the waveguide is the radiation losses at the bending sections of the waveguide. For the waveguides fabricated from the

positive pattern as described in Figure 2.7, we have fabricated semicircular waveguides which has a bending loss of 0.22 to 0.66 dB per semicircle. After optimizing the pre-clean step and the dry etching to get smooth sidewalls we have been able to further reduce it to 0.11 to 0.33 dB per semicircle. The structures used for the fabrication of the bending loss are shown in Figure 2.10.

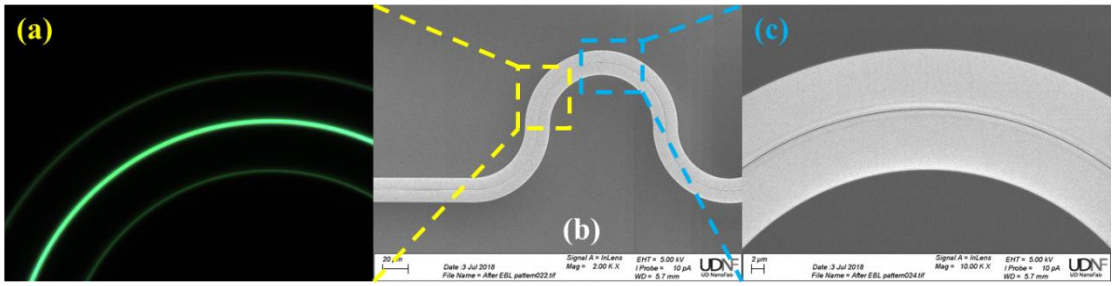

Figure 2.10 – (a) Dark field image of the bending section of the wire waveguide showing no defect or breakage (b) Top view of the SEM of the bending section used for calculating bending loss (c) Magnified SEM image of the bending waveguide

2.3 Diffraction Grating Couplers

Fiber-chip coupling is a very integral part of the successful integration of nanophotonic components to electronics. To couple the infrared light from the external optical fiber to the waveguide we need couplers which have low loss, lesser light leak and efficient coupling. These passive devices which couple the light into the waveguide are called Couplers. There are different methodologies to couple light namely edge or vertical coupling. In our experiments, we have only used vertical coupling using different designs of couplers namely rectangular diffraction grating coupler with a taper and confocal type grating coupler. Diffraction grating has been preferred since they are alignment tolerant, broadband and polarization independent.

Also, it eliminates the necessity of cleaved and polished surface required for edge coupling. An example of the fabricated diffraction grating coupler for our photonic chip is shown in the SEM picture in Figure 2.11.

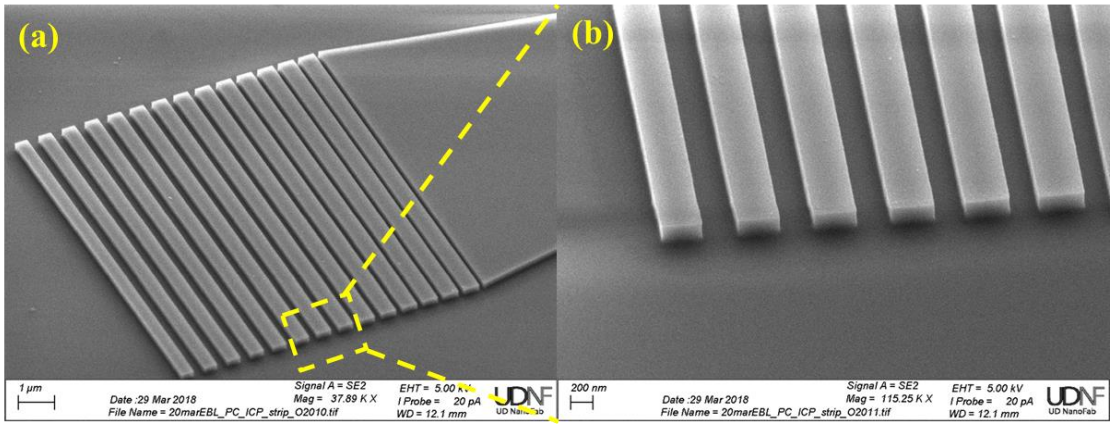

Figure 2.11 – (a) Tilted angle SEM of Diffraction grating coupler with taper
(b) Magnified view of the grating showing vertical edges

A diffraction grating consists of one-dimensional periodic structure which diffracts light in preferential directions. The scattering from the periodic structure results in a strong angle-dependent interference which follows Bragg's law. For light coupling, we select the grating period in such a way that there is only a single order of diffraction to channel light into the waveguide. Though gratings are highly polarization sensitive to transverse electric and transverse magnetic field since they have different diffraction angle there are design considerations to be made to make the grating broadband. However, in this section, we will discuss more about the issues with respect to the fabrication of these couplers rather than the design problem.

2.3.1 Experimental Realization of Diffraction Grating Coupler

In Figure 2.12 and 2.13 we have shown the 2 different types of grating coupler that we have used in our layout. We have also tested the loss in these couplers which would be explained in the next sections. The fabrication method of these couplers is similar to the method described in section 2.1.

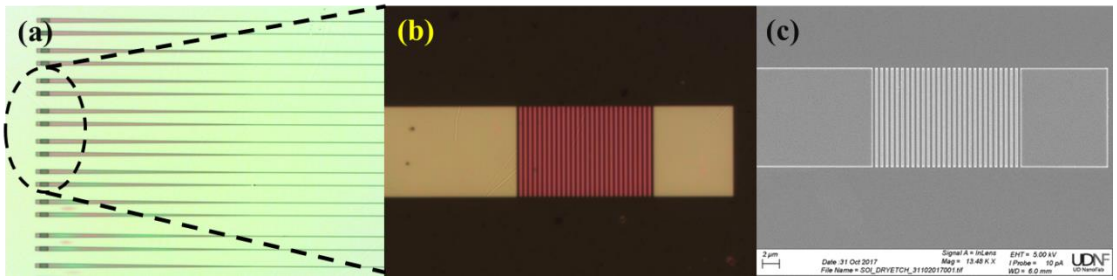

Figure 2.12 - (a) Layout of the rectangular diffraction grating coupler with taper used for measuring loss (b) Optical image and (c) SEM top view of the rectangular diffraction grating coupler

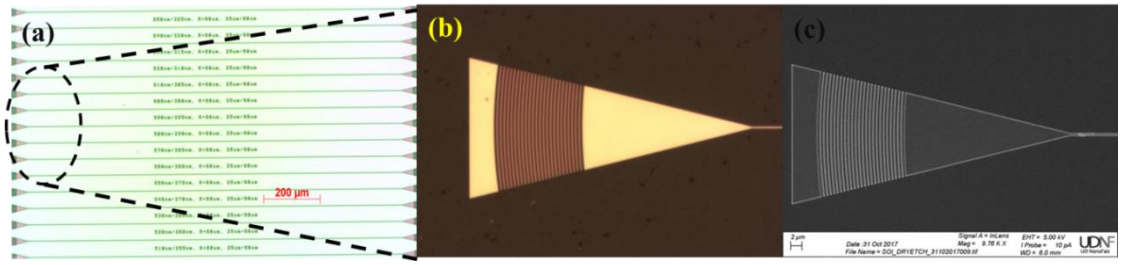

Figure 2.13 - (a) Layout of the confocal diffraction grating coupler used for measuring loss (b) Optical image and (c) SEM top view of the confocal diffraction grating coupler

One of the issues faced during the fabrication of the coupler is the development of the pattern on the photoresist. Careful optimization is needed to prevent either under-developed or over-developed condition. Also, the development time which is

usually done on larger features might be different for the coupler due to the micro-loading and high aspect ratio. In Figure 2.14 we can see under-developed regions between the coupler. A possible reason for this could be the developer solution has lesser solubility due to the high concentration of pattern leading to micro-loading effect or the E beam scattered around the high-density pattern causes partial exposure of the adjacent resist changing its solubility.

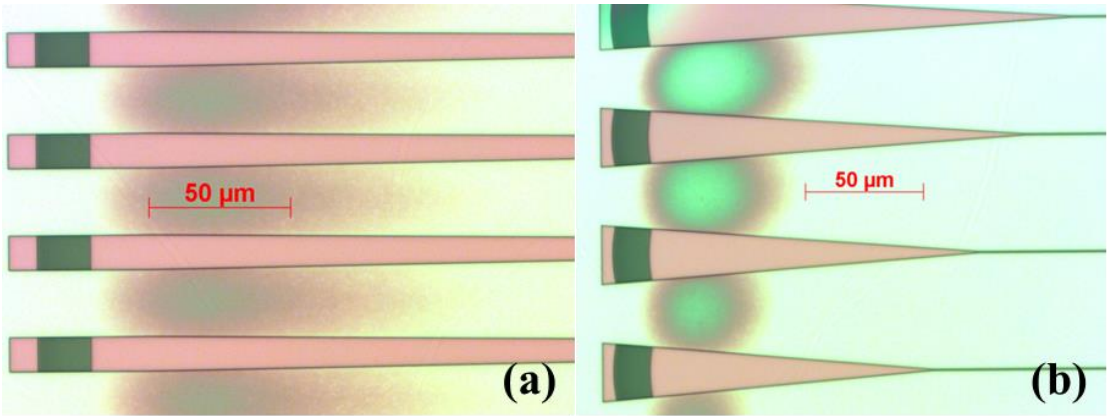

Figure 2.14 – Optical image of the underdeveloped region (a) rectangular diffraction grating coupler (b) Confocal diffraction grating coupler

This problem has been overcome by optimizing the development time to develop the additional under-developed region. The predicted thickness of the resist from the spin curve is ~400 nm and the actual thickness measured by dektak profilometer was ~380 nm. After development, the thickness of the underdeveloped region was ~60 nm. Therefore the development time was increased by an additional 20 seconds, from 90 to 110 seconds. We can thus see in Figure 2.15 that there are no underdeveloped regions in the optical or SEM image near the grating.

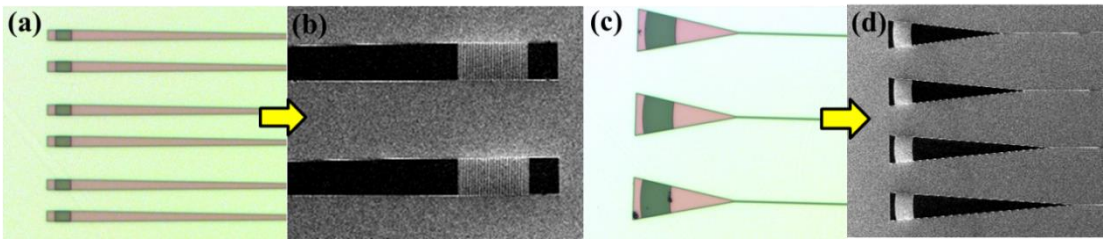

Figure 2.15 – (a) Optical light microscopy and (b) SEM image of Rectangular diffraction grating coupler. (c) Optical light microscopy and (d) SEM image of Confocal diffraction grating coupler

Another method to remove the under-developed region was to use the positive pattern transfer described in section 2.2.1. The pattern transfer is shown in Figure 2.16. We can clearly see that there are no underdeveloped regions near the coupler and there is a clean transfer of the pattern on the chip.

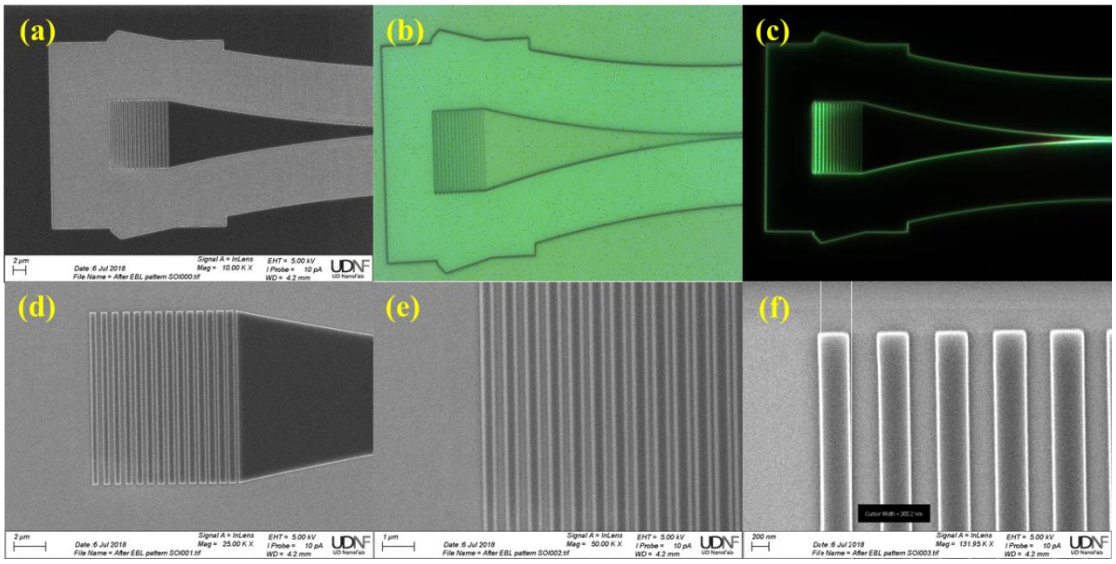

Figure 2.16 (a) Top SEM view (b) light field (c) dark field (d)-(f) magnified SEM of diffraction grating coupler using positive pattern transfer

2.3.2 Diffraction Grating Coupler Characterization

For the rectangular diffraction grating coupler using negative pattern transfer, we have got the lowest propagation loss of -25 dB at a wavelength of 1506 nm. Similarly, for the patterns made with positive pattern transfer, the lowest propagation loss is -17.86 dB. It is important to note that all the structures have a silicon oxide cladding layer deposited by PECVD. On an average, we got a propagation loss of -6 to -8 dB/cm and grating coupler loss of less than -10 dB/cm per facet.

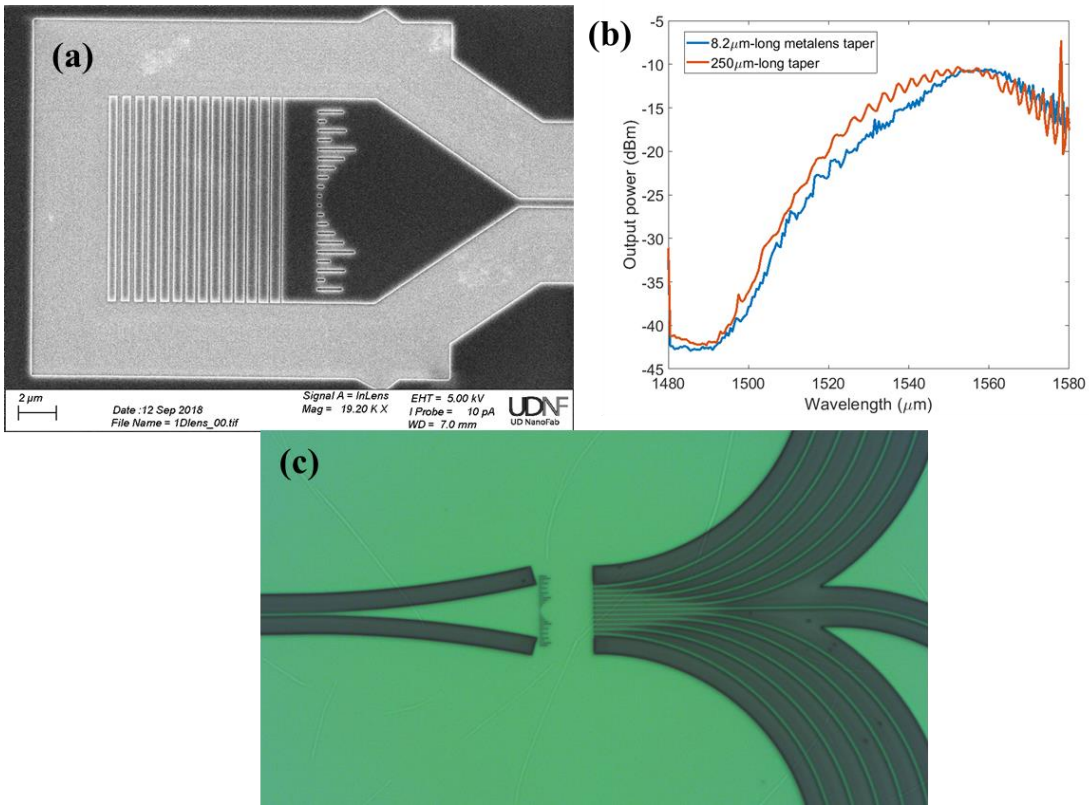

Figure 2.17 – (a) Top view SEM of diffraction grating and ultra-short metal lens taper (b) Measured output power spectrum of conventional 250 μm taper versus 8.2 μm metal lens taper (c) Optical light field image of meta-lens structure used for its characterization

(Credit: Zi Wang)

After fabricating the standard diffraction grating we have used these recipes for some advanced concepts like making low loss on-chip lens with high contrast dielectric meta-surface [4]. The fabrication methodology developed has been used to make metamaterial lens which can achieve broadband and dispersionless wavefront shaping. Figure 2.17.a shows a meta-lens taper comparing its performance with a conventional taper and find similar output power spectrum. Thus we have obtained highly compact on-chip meta-lens taper the details of this work will be published in our future work.

2.4 Micro-Ring Resonator

Ring resonators are a specialized type of waveguides which couple light into a closed loop to manipulate light by the phenomenon of resonance. A closed loop (ring) waveguide adjacent to a waveguide will couple light into it due to the evanescent field of the wave which extends outside of the waveguide. This coupled light wave undergoes multiple passes within the loop increasing the intensity by constructive interference. If the superimposing waves interfere constructively, at certain wavelength they create a resonance which underlies the basic principle of a Micro-ring resonator. Since resonance only happens at a certain wavelength ring resonators act as an optical filter which finds application in many photonic circuits [5]. In this section, we will discuss the fabrication process and optimization methods for micro-ring resonators.

The fabrication process is similar to the generic procedure discussed in section 2.1. Only the additional optimization steps and the results are emphasized here. Figure 2.18 shows the SEM image of a micro-ring resonator fabricated highlighting the

different critical dimensions of the resonator. From the fabrication point of view, the 2 critical parameters which affects the optical coupling is the gap length between the ring and the waveguide and the dimension of the ring (coupling length). Therefore we will discuss a few points which need to be checked during the fabrication process. There is one another parameter which is of utmost importance i.e. the surface roughness. Since we have already covered that during the discussion of section 2.2.1 stating the optimization steps for solving it, we will only talk about the other 2 factors.

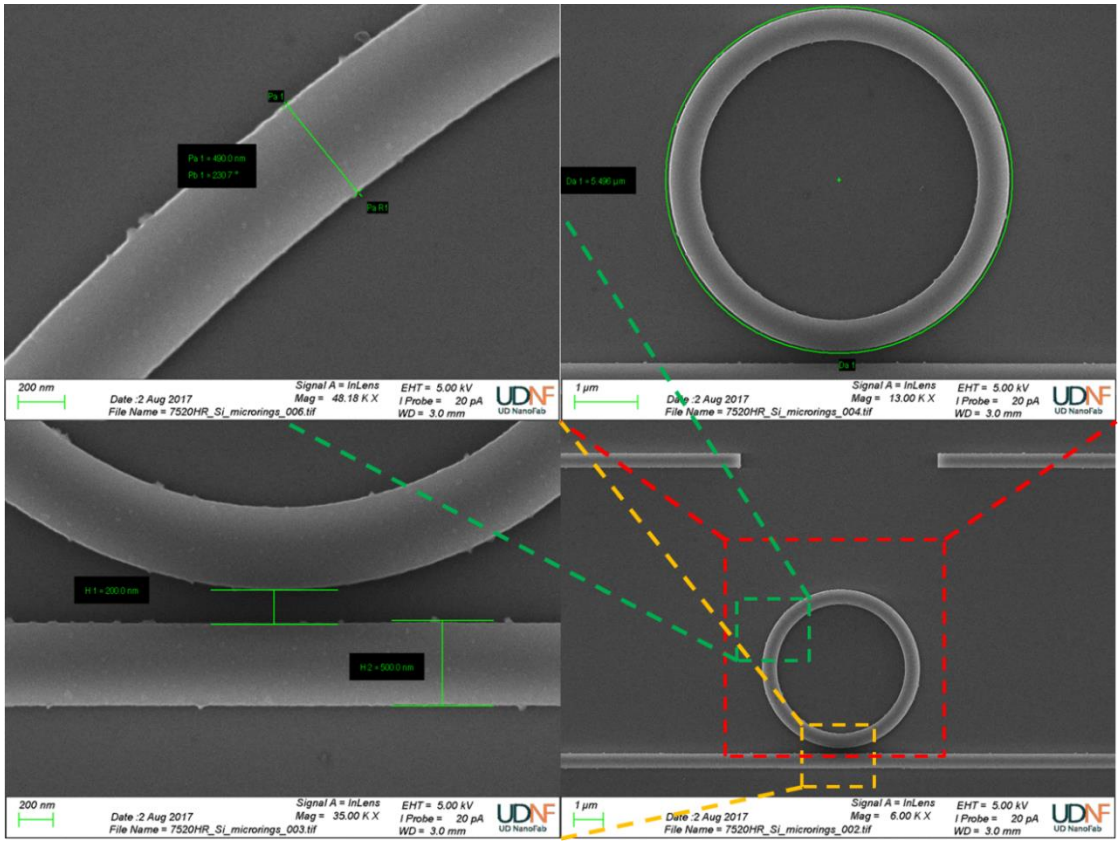

Figure 2.18 – Top view SEM of a Micro ring resonator fabricated, the different sections shows magnified view of the waveguide, ring and gap between the ring and waveguide to show the dimensions of the fabricated structures

For fabricating Micro-ring resonators we can use both the positive as well as negative pattern transfer discussed previously. However, most of our results in this section are for the negative pattern transfer process described in section 2.1. Additionally, we do a descum process before ICP etching for 30 seconds in oxygen plasma to remove any additional photoresist in the trenches of the microring. This step is important since the gap length is usually very small of the order of 200 nm so the developer solution sometimes does not dissolve the resist in such a small gap size. Therefore we have found that such a descum step helps remove any such residue which hasn't been removed by the developer. For similar reasons, we do an NMP cleaning of the sample after ICP etching to dissolve any resist residue from the small gap between the micro-ring and the waveguide. In Figure 2.19 we can see the resist residue remains on the structure due to the poor development process and when these additional steps to completely remove the resist are not performed.

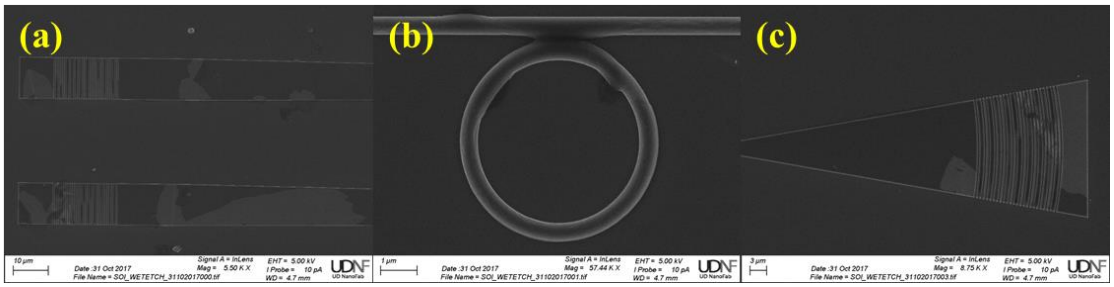

Figure 2.19 – Photoresist residue remains on (a) rectangular diffraction grating coupler (b) Micro-ring resonator (c) confocal diffraction grating coupler due to poor development process

In Figure 2.20 we have done the additional steps of descum and NMP cleaning previously discussed and we can see that there are no residue in the SEM of the microring structure. We also observed the structure under a dark and light microscope

to detect any particulate remains or breakage and found there was a clean pattern transfer. After the fabrication of the ring, we deposit a 1 μm of SiO_2 at 300 °C using 360 sccm SiH_4 + 1080 sccm N_2O+ 1400 sccm of N_2 at 1.4 Torr as cladding layer for optical confinement. After the cladding layer, we have characterized these ring resonators for their performance.

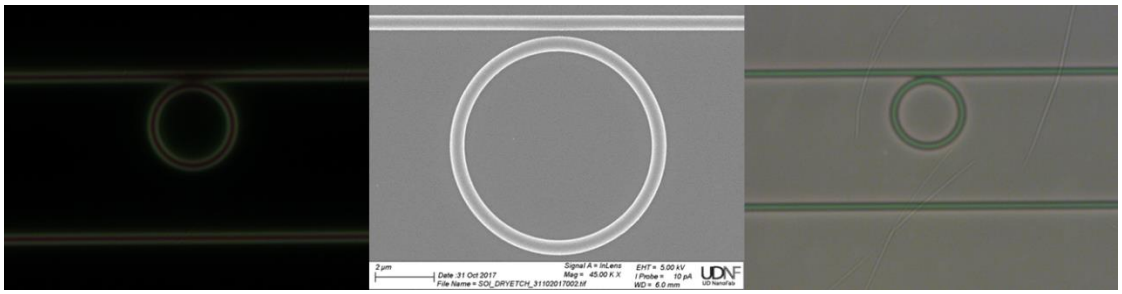

Figure 2.20 – (a) Dark field (b) SEM (c) Light field image of Micro-ring resonator after additional descum and NMP clean step showing no resist residue

After fabricating the ring resonator we have characterized them by measuring its transmission spectra as shown in Figure 2.21. When we do a wavelength scan to measure the transmission of the ring resonator we basically find two phenomenons. First, if the wavelength of light wave coupled into the ring is off resonance then the light wave is rejected by the ring hence gets transmitted. However, if the wavelength of light wave coupled into the ring is in resonance then they get dissipated by the ring and are not transmitted, this results in a dip in the spectra as can be observed in Figure 2.21. The wavelength range between 2 resonances is called Free Spectral Range (FSR) and to a first order of approximation the FSR can be defined as [6]:

$$\mathrm{FSR} = \frac{\lambda^2}{\mathrm{n.L}} = \frac{\lambda^2}{\mathrm{n}\,(2\pi \mathrm{r})}$$

where λ is the wavelength of light wave (usually 1550 nm for telecommunication applications), n – refractive index of the material of waveguide, L – round trip length, r – radius of the micro-ring. Therefore for our structure where λ = 1550 nm, n = 3.5 (refractive index of silicon – at 1550 nm), r = 4μm, FSR is ~23 nm. The transmission spectra in Figure 2.21 show multiple dips due to a short FSR ring resonator. The minimum propagation loss observed in this ring resonator is -28.52 dB. The Q factor (Quality Factor) which is the measure of the sharpness of the resonance relative to the central frequency of the peak is given by the formula:

$$\text{Q factor} = \frac{\lambda}{\text{FWHM}}$$

where λ is the wavelength corresponding to central frequency and FWHM is the full-width half maximum of the transmission dip at the central frequency. To calculate the Q factor we have taken the data from graph 2.21 at a central wavelength 1549.6 nm and we found the Q factor to be 26000. After successfully fabricating and characterizing these ring resonators we have used them for advanced applications like having a notched microring resonator which helps in partial coupling of the counter-propagating wave by introducing a small perturbation in the form of a notch [7]. The scattering loss introduced by the notch helps the ring resonator to act as a second order filter [8]. The initial result of the fabrication of the notched ring resonator is given in Figure 2.22 and a detailed characterization along with its theory will be provided in our future work.

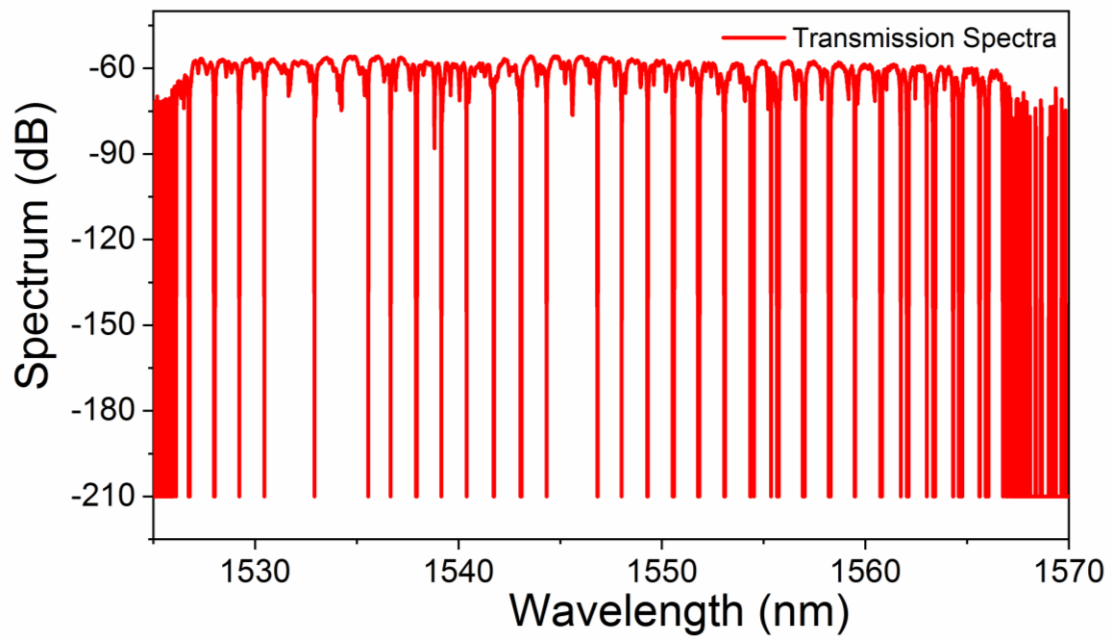

Figure 2.21 – Transmission Spectra of Microring resonator

(Credit: Dun Mao)

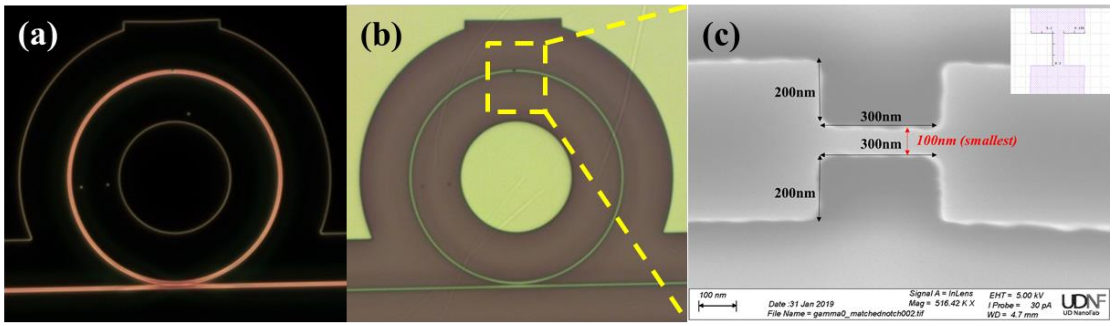

Figure 2.22 – (a) Dark field (b) Bright field and (c) SEM of Notch ring resonator

(Credit: Hwaseob Lee)

2.5 Photonic Crystal Waveguide

Photonic crystals (PC) are structures which can confine light due to photonic bandgaps [9] which arise from the index contrast. Thus a two dimensional (2D) PC waveguide (PCW) can help in horizontal confinement of light due to index guiding in a slab waveguide. PCW provides strong dispersion resulting in slow-light effect [10]. This slow light phenomenon enhances absorption, non-linearity and provides strong light-matter interaction which finds application in a wide range of photonic devices like photodetectors, modulators, amplifiers, lasers and sensors. In this section we will discuss only about the fabrication constraints of PCW and solutions to overcome it.

Just like the previous section, PCW follows the standard fabrication process discussed in section 2.1. The additional steps which are specific to PCW and the reasons for having these steps are elucidated in this text. Since the feature size of the cavities of PCW is of the order of hundreds of nanometers the process of development and etching are very critical. Development process is important and should be performed with care to prevent under or over development. Under developed condition results in cavities not being developed and overdeveloped condition results in a floating pattern or complete removal of the pattern. Due to the small feature size, it is difficult to completely remove the resist from the cavities. Therefore, just like the additional process steps in ring resonators we need to perform a descum and NMP clean as previously discussed. A common problem observed as can be seen in Figure 2.23.a and 2.23.b is the hardening of the resist after ICP etching. For this we do an additional step for resist stripping from the cavity using AR-300-76 at 80 °C sonicated at 192 kHz. We strip the hardened resist on the PCW sample in AR 300-76 stripper (designed for 7520 resist) at 80°C for 2 hours. It is important to note that stripping the sample only in AR 300 76 results in residual resist. We also sometimes observe

residual resist in the cavities as shown in Figure 2.23.c. At this stage, if the resist isn't completely removed then we soak it in NMP solution at 80°C till the resist is completely removed as can be observed in Figure 2.23.d. On an average it takes about 2-3 hours of wet etching in NMP for complete residue removal.

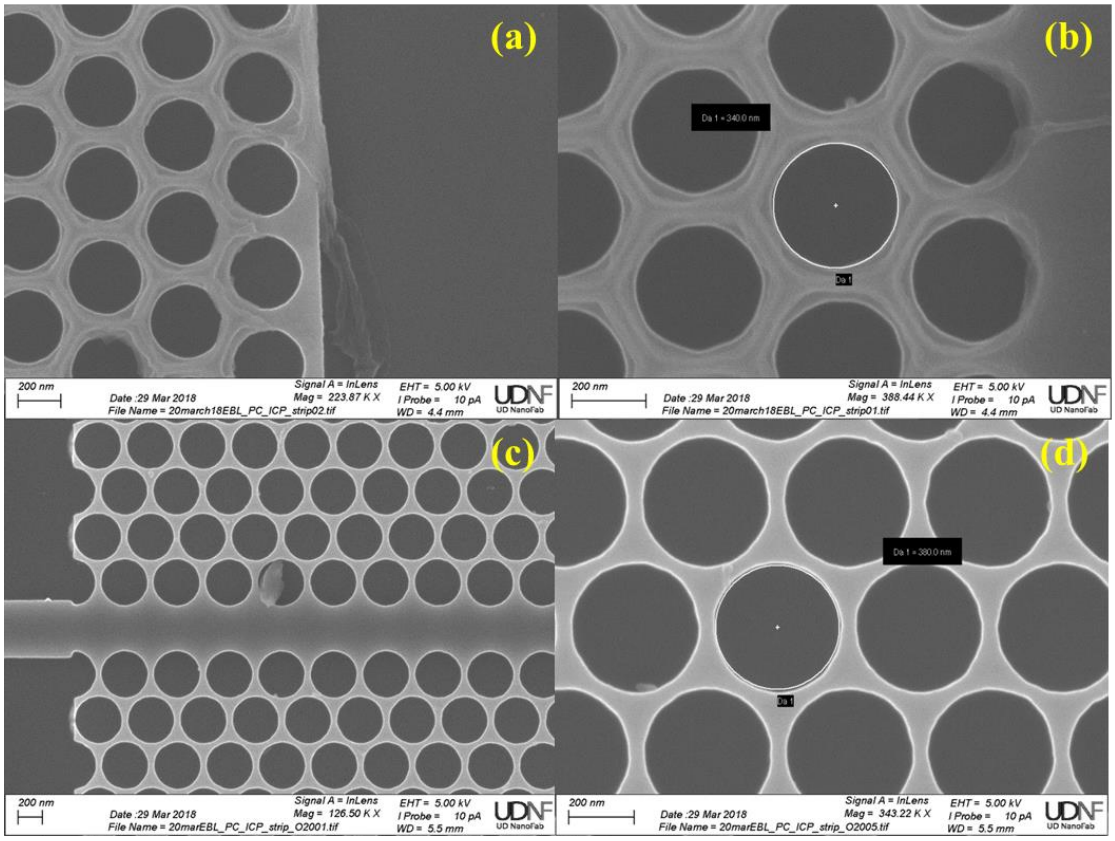

Figure 2.23 – SEM of (a) & (b) photonic crystal (PC) waveguide showing hardened photoresist (c) Residue of resist in pits of PC waveguide (d) PC waveguide after resist removal

After complete removal of the residual resist, we do the final plasma ashing to get clean PCW as seen in Figure 2.24. Occasionally, we sometimes observe a side wall collapse of the PCW, this is due to the thin edge of the PC sidewall (~30 nm) as can be seen in Figure 2.24.c. For this, we have used a reduced thickness of the resist from 400

nm to 200 nm. We spin-coated with negative resist AR-N-7520-18 for a new thickness of 200 nm and followed all the other steps of development previously discussed. Also for complete resist removal, we kept the PCW sample in NMP solution at room temperature overnight (~24 hours) followed by a 2 step plasma ashing for 10 minutes each. No hardened resist was observed after the double ashing step and the final devices fabricated are shown in Figure 2.25.

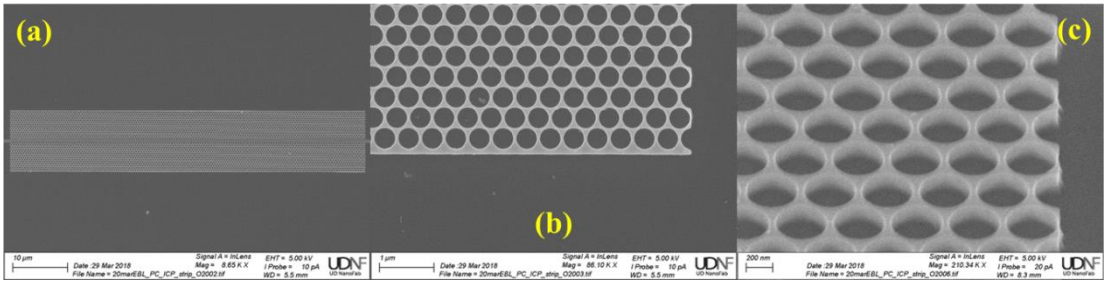

Figure 2.24 – SEM top view of (a) & (b) PC waveguide after etching (c) tilted angle view showing edge collapsing

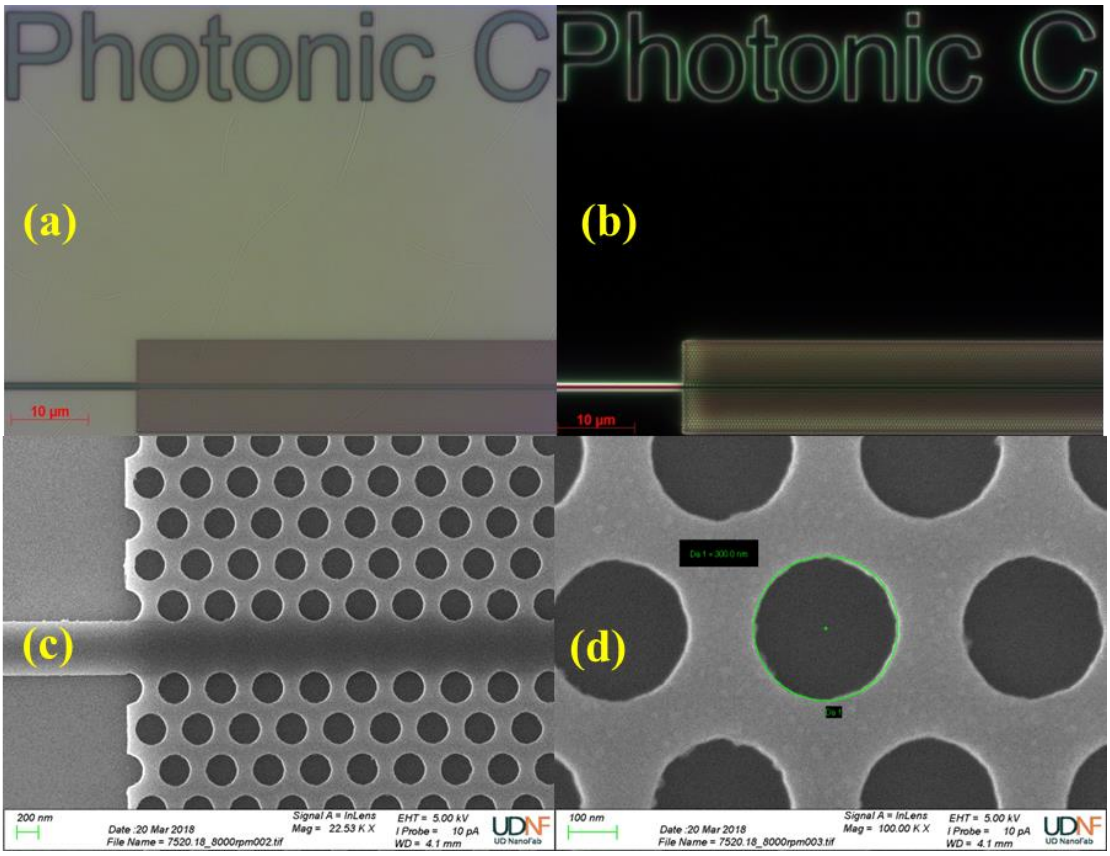

Figure 2.25 – (a) Bright field (b) Dark field (c) SEM of PC waveguide. (d) High resolution SEM of PC waveguide showing the dimension of the cavity to be exactly 300 nm.

Chapter 3

FABRICATION OF MATERIALS FOR NANOPHOTONICS

3.1 Amorphous Silicon (a Si: H)

Amorphous Silicon (a-Si: H) is a widely used and commercially feasible material used in the microelectronic industry. However, due to its high defect density, it has found limited application in Photonics. However though a-Si: H has been less explored in the photonic industry it has high potential due to its lower cost, high non-linearity, lower non-linear absorption and ease to integrate with current industrial technology. The reason it could possibly find applications in photonic industry is that it has higher optical non-linearity and lower non-linear absorption as compared to crystalline silicon. The bandgap of a-Si: H is ~1.8eV which means that it is transparent in the near-infrared range used for telecommunication and computer signaling applications. The absorption loss at this infrared wavelength (1300 to 1550 nm) is only dependent on defects due to the dangling bonds in the a-Si: H amorphous matrix. To obtain a lower defect density we have developed advanced hydrogenation techniques to passivate the dangling bonds [11]. A low loss a-Si: H required for photonic application need to be well passivated to have minimum losses due to defects. The low propagation loss can be achieved by passivating the dangling bonds in the amorphous matrix by hydrogenation while depositing the films. This section will discuss the process of fabricating high-quality amorphous films and the results of the photonic components fabricated out of it.

3.1.1 Fabrication Process of a-Si: H Photonic Components

High-quality a-Si: H thin films needed for fabrication of waveguides were deposited using d.c. plasma enhanced chemical vapor deposition (PECVD) using Silane (SiH_4) and hydrogen (H_2) as the precursor gases at a temperature of 200 °C. The chamber pressure was maintained at 1750 mTorr and the SiH_4 to H_2 gas dilution was 2:5. The etching of a-Si: H is done using ICP RIE etch tool previously explained before and the etch rate was calculated to be 6.5nm/sec. We deposited ~250 nm of a-Si: H for fabricating the waveguides. One of the primary issue faced during fabrication of a-Si: H devices is the adhesion of the a-Si: H patterns on glass similar to the issue shown in Figure 2.1. To resolve this issue we have tried 2 approaches. One is mainly using an adhesion promoter and the other is HMDS. We have used adhesion promoter AR-300-80 which was spin coated at 4000 rpm for 1 minute then baked at 180 °C for 2 minutes. The other approach was treating with HMDS (hexamethyldisilazane) at a Pressure of 1000 mTorr and Temperature of 150 °C. The details of both have been previously explained and we found that the adhesion promoter was a better approach to avoid waveguide breakage.

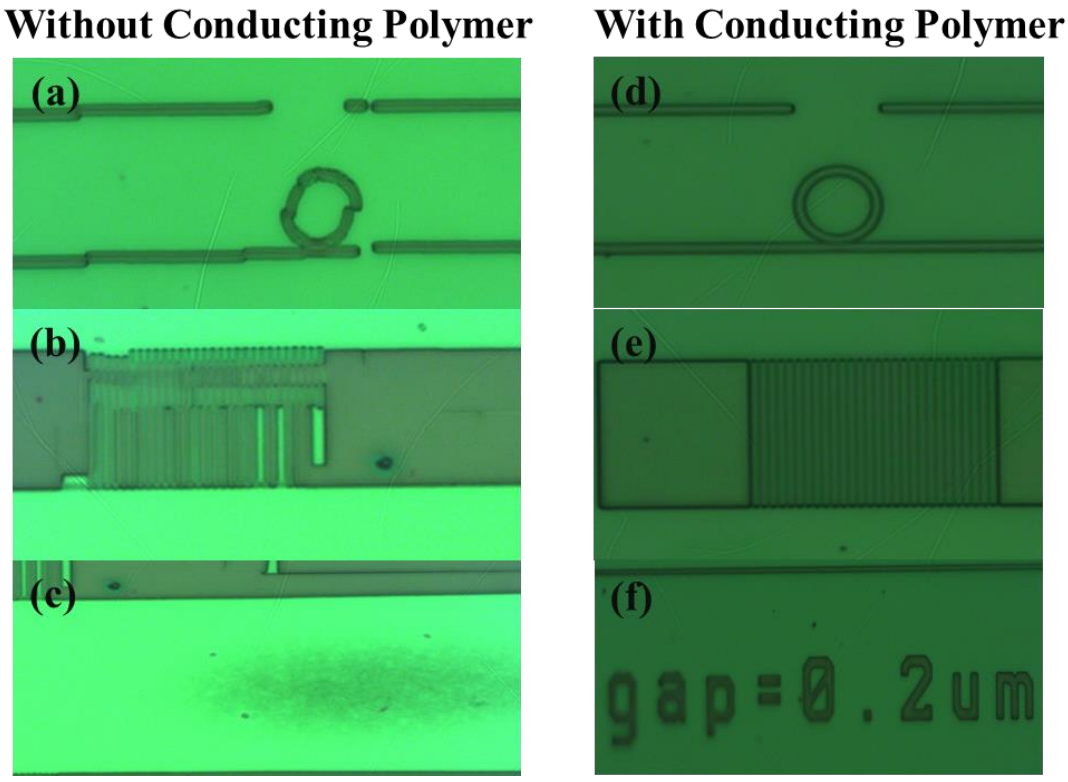

Figure 3.1 – (a-c) Optical image of pattern transfer without conducting polymer (d-f) image of pattern transfer with conducting polymer

Another problem we faced after the development of the pattern was deformation and misaligned pattern transfer as can be seen in Figure 3.1 a to c. The transfer of pattern was very poor on the resist. In order to remove the possibility of problems with EBL, the same pattern was written on a c-Si wafer which has undergone the same procedure and we found that the process or the lithography step did not have any problem. After troubleshooting, we realized this could be due to the charging of the substrate due to the poor conductivity of the sample. To resolve the charging problem we spin coat the sample with conducting polymer (AR-PC-5091-02) 2000 rpm for 1 minute then baked it at 50 °C for 2 minutes. The conducting polymer

spin-coated on the substrate helps to remove the charging effect. Thus the conducting polymer helped to overcome this issue of poor pattern writing on a-Si: H with improved pattern transfer as can be seen in Figure 3.1 d to f.

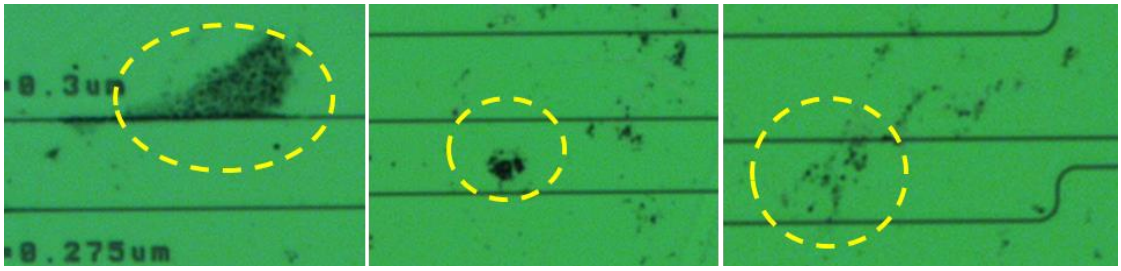

Figure 3.2 – Residue remains on a-Si:H patterned substrate after development process

By adding the additional conducting polymer step we found that there were residue remains on the surface after development. The possible source of this residue was the remains from the newly introduced polymer step. Therefore to skip using the conducting polymer we also tried a very thin layer of chromium (Cr) deposition on the sample which removed this problem. However thermal evaporation of Cr brings in additional steps of thermal evaporation and Cr etching which increases the number of steps, time as well as fabrication cost. Therefore we tried to resolve the issue of residue removal from conducting polymer. We found that DI water rinse before development can help to remove any residue of the conducting polymer. It can be clearly seen in Figure 3.3 that thorough rinsing of sample in DI water followed by an additional sonication in DI water before development can completely remove the residue. Note that before lithography it is also important to clean back surface with

NMP so that any resist residue from the chuck on the back, which is usually ignored, does not cause any height variation during lithography.

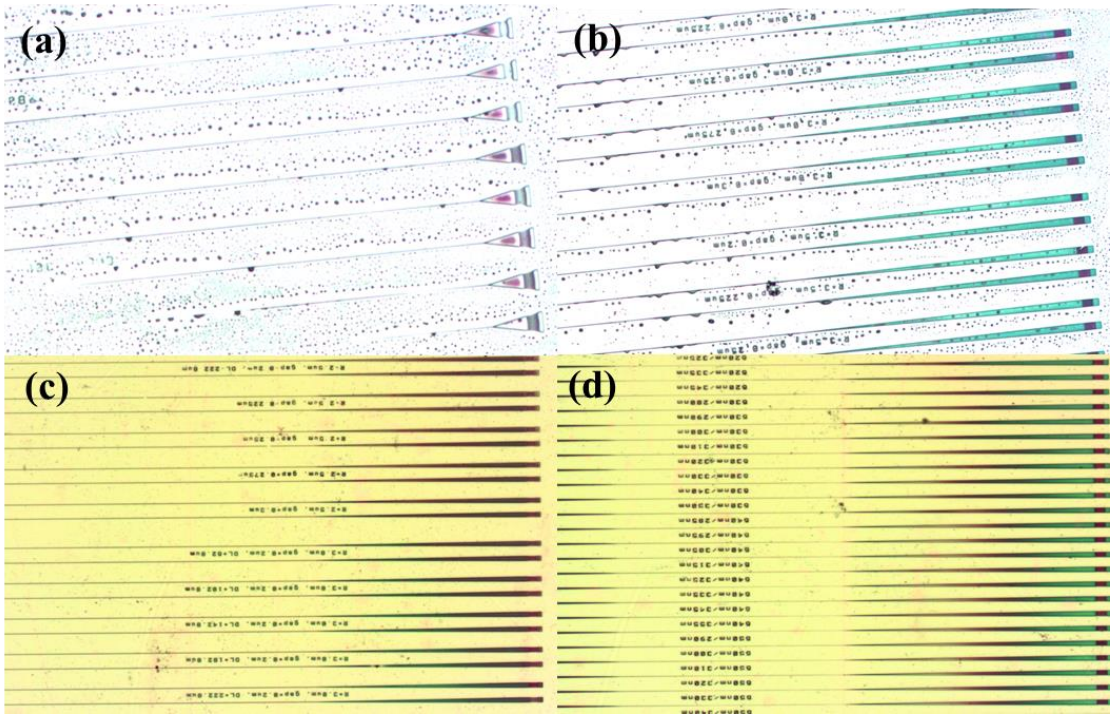

Figure 3.3 – (a-b) Pattern with conducting polymer residue (c-d) Pattern after DI rinse before development completely removing polymer residue

After resolving these additional problem in the fabrication of photonic devices using a-Si: H we made the first prototype structures on glass. The structures fabricated are shown in Figure 3.4 and includes waveguides, ring resonators, grating couplers and photonic crystal waveguides. As can be seen in the SEM pictures we have had good pattern transfer just like structure on c-Si. However, the devices were lossy with ~50 dB propagation loss which needs to be optimized and will be presented in our future work.

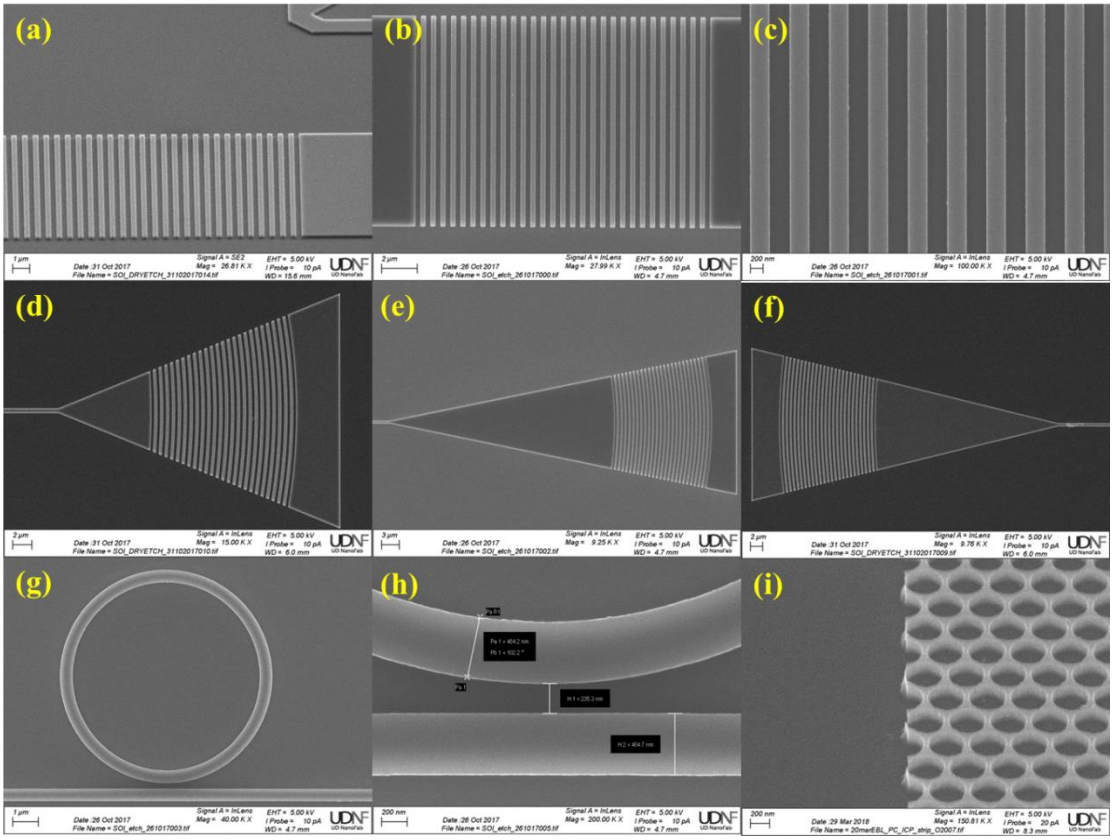

Figure 3.4 – SEM of (a-c) Rectangular diffraction grating coupler (d-f) confocal grating coupler (g-h) micro-ring resonator (i) photonic crystal waveguide for a-Si: H photonic platforms

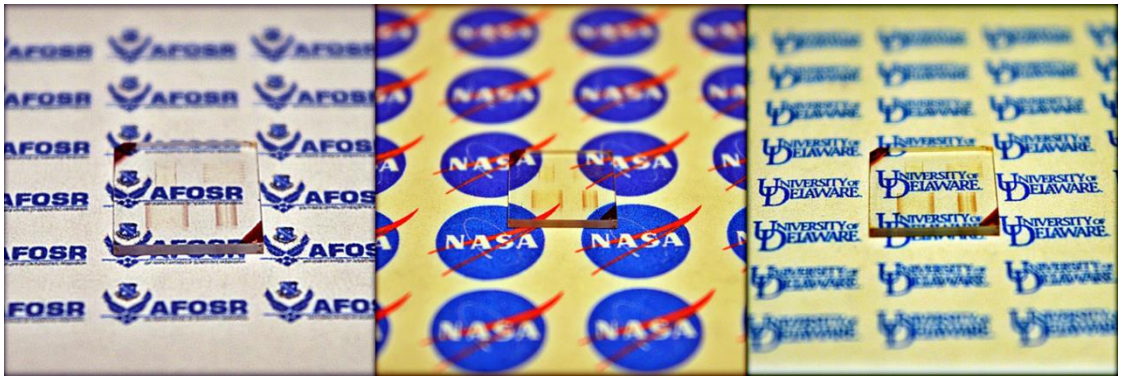

Figure 3.5 – Pictures of first prototype a-Si: H photonic devices fabricated on glass in our Nanofabrication cleanroom (UDNF)

3.2 Amorphous $Ge_2Sb_2Te_5$ (GST)

Germanium Antimony Telluride (GST) is an amorphous chalcogenide material widely used in electronic and optical devices due to its phase changing properties i.e. it can be reversibly transformed from amorphous to crystalline phase on application of thermal energy [12]. Like most chalcogenide material GST has distinguishable properties in different states which we will be studying in this section. Due to its phase changing properties GST has found application in non-volatile memory, optical recording etc. The change in state of GST can be done thermally using an electrical or optical pulse like a laser source which can create localized heating to change the GST between amorphous to crystalline phase. The crystallization temperature of the alloy is between 100 to 150 °C. It has been previously studied that at GST transitions from amorphous to crystalline phase (Face-centered cubic structure – fcc) at ~150 °C. And it transitions from fcc to hexagonal closed pack (hcp) structure at ~230 °C. Therefore in order to study the different phase properties of GST we have deposited GST at room temperature (RT), 150 °C and 225 °C using physical vapor deposition methods. In this study, we have used thermal evaporation to deposit GST and the tool used for its deposition is shown in Figure 3.6.

The thermal evaporator chamber is shown in Figure 3.6.a. The chamber is connected to a roughing pump and a turbo-molecular pump to achieve a high vacuum. The front panel of the system is shown in Figure 3.6.e from where we turn on the chiller for cooling the chamber, roughing pump and the high vacuum gauge. We load the sample onto the substrate holder seen in Figure 3.6.f which has a filament heating unit for substrate heating. The substrate heater can be changed from the controller shown in Figure 3.6.b. The powdered GST is loaded on the Molybdenum (Mo) boat shown in Figure 3.6.d. After loading the sample, boat, heating the substrate and

pumping down the chamber to ~100 mTorr by roughing pump we open the gate valve and pump down the chamber to high vacuum using the turbo-molecular pump. This opens the interlock for ion gauge which reads the pressure as shown in Figure 3.6.c and we do the deposition at ~1 x 10^{-6} Torr. The power and deposition rate is controlled by the deposition controller by Inficon as shown in Figure 3.6.g. The power is gradually increased from 11% to 20% maintaining a constant deposition rate. Thus GST of desired thickness is deposited.

Figure 3.6 – (a) Evaporator chamber (b) substrate heater controller (c) High vacuum gauge (d) Mo boat (e) Front control panel (f) Substrate holder and filament heater (g) Deposition controller

3.2.1 Characterization of GST

In order to understand the phase change properties of GST we have characterized the GST films deposited at different temperatures namely room temperature (RT), 150 °C and 225 °C and the results are presented below.

The surface morphology of the evaporated GST film is shown in Figure 3.7. The SEM of the surface of GST at RT is almost atomically flat and no features are observed as shown in Figure 3.7.a. To re-verify if the surface morphology is flat with no features an Atomic Force Microscopy (AFM) image of the surface was taken which helps us determine the root-mean-squared roughness (R_{RMS}). R_{RMS} is given by the standard deviation of the z-values for the sample area scanned by the cantilever of the AFM. Because the RMS roughness (σ) contains square terms of the z height, large deviations from the average height are weighted more heavily than that for the mean roughness. The σ value might have influence of large particles, therefore, area of the scan was reduced to 5 x 5 μm as shown in Figure 3.7.b to d. We find that σ decreases from ~1 nm to 0.25 nm when the substrate temperature increases from RT to 150 °C. Even at 225 °C, the value of σ is only about 0.5 nm. Thus increase in the substrate temperature decreases the surface roughness of the films and the overall rms roughness of the evaporated films does not exceed 1 nm making it suitable for waveguide application in photonics.

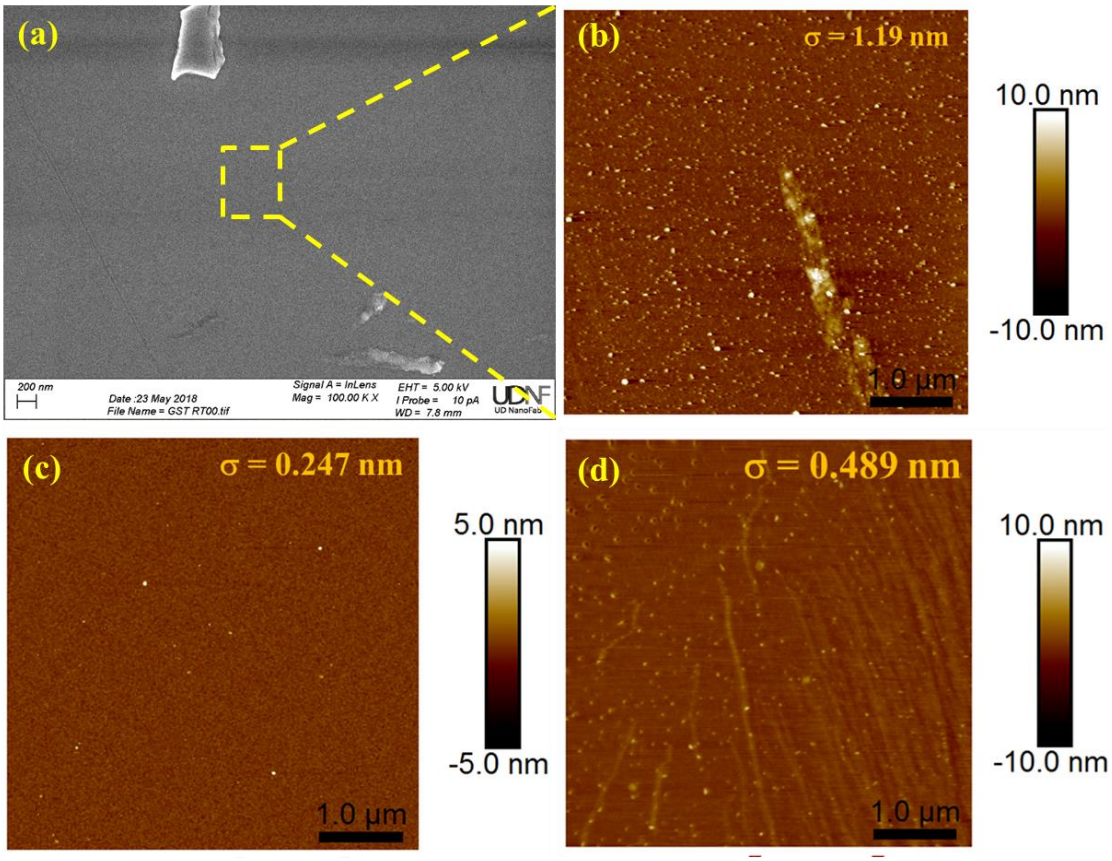

Figure 3.7 – (a) Top view SEM of GST at RT. AFM image of (b) GST at RT (c) GST at 150 °C and (d) GST at 225 °C

In order to understand the crystalline nature of GST, we measured the X-ray Diffraction (XRD) of the thin films grown at different temperature. The result of the XRD is shown in Figure 3.8.a. The XRD in 3.8.a shows no characteristic crystalline peak in any of the thin films. XRD wasn't able to determine the crystalline nature of GST due to the higher penetration depth of incident rays. We assumed a probable reason would be that the X-ray is penetrating the film which is only ~50 nm and the signal is coming from the amorphous phase of the glass showing a broad peak. Therefore we tried the Grazing angle incidence measurement which performs small angle measurement the result of which is shown in Figure 3.8.b. Grazing angle

measurement was done with incident angle of 0.5° for θ = 20° to 50°. An inbuilt software – Absorb DX was used to find the depth of penetration for Grazing angle of 0.5° at the highest peak position of 30° for GST, this is because the cubic structure of $Ge_2Sb_2Te_5$ has the biggest peak at ~ 30°. It was found to be ~ 80 nm which was within the thickness limit of the sample (~ 50 – 60 nm) which increases the reliability of the data. All 3 films show amorphous bump at ~ 28 ° showing the absence of any crystalline fraction in the film. Thus it wasn't possible to detect any crystalline phase from the bulk of the material using XRD.

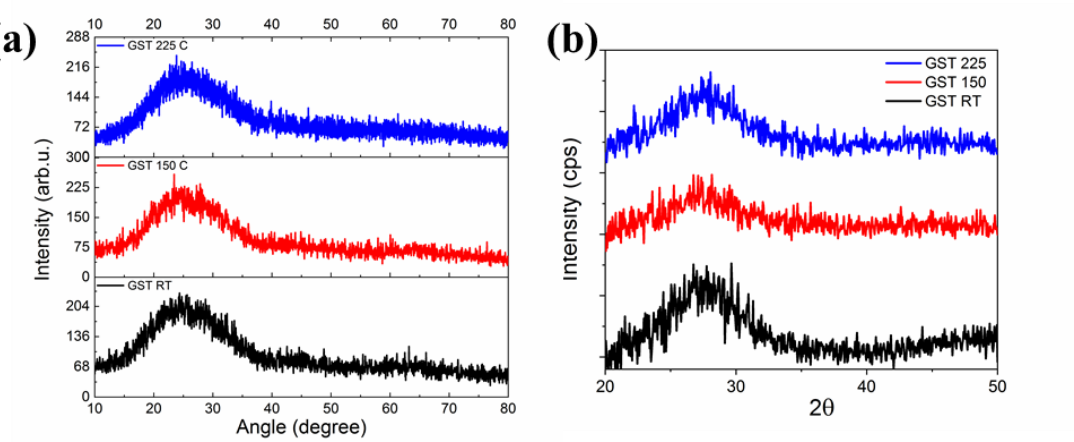

Figure 3.8 – (a) XRD of GST deposited at different temperature (b) Grazing angle XRD of same thin films

The optical characteristics of the GST can be obtained from UV-VIS-NIR (Ultraviolet-Visible-Near-infrared) Spectrophotometer. The reflection (R), transmission (T) and absorption (A) spectra of GST films are important for its application in optical or photonic circuits. The R, T and A data for different GST films are shown in Figure 3.9.a to c. We find that the substrate temperature does have an effect on the optical properties of the GST films with the film deposited near the

crystallization temperature at 150 °C showing an anomaly as compared to the other 2 films. The refractive index (n) and extinction coefficient (k) of GST were measured by an ellipsometer. At 1550nm, GST has n=3.83 and k=0.044 as shown in Figure 3.9.d. (Credit: Dun Mao)

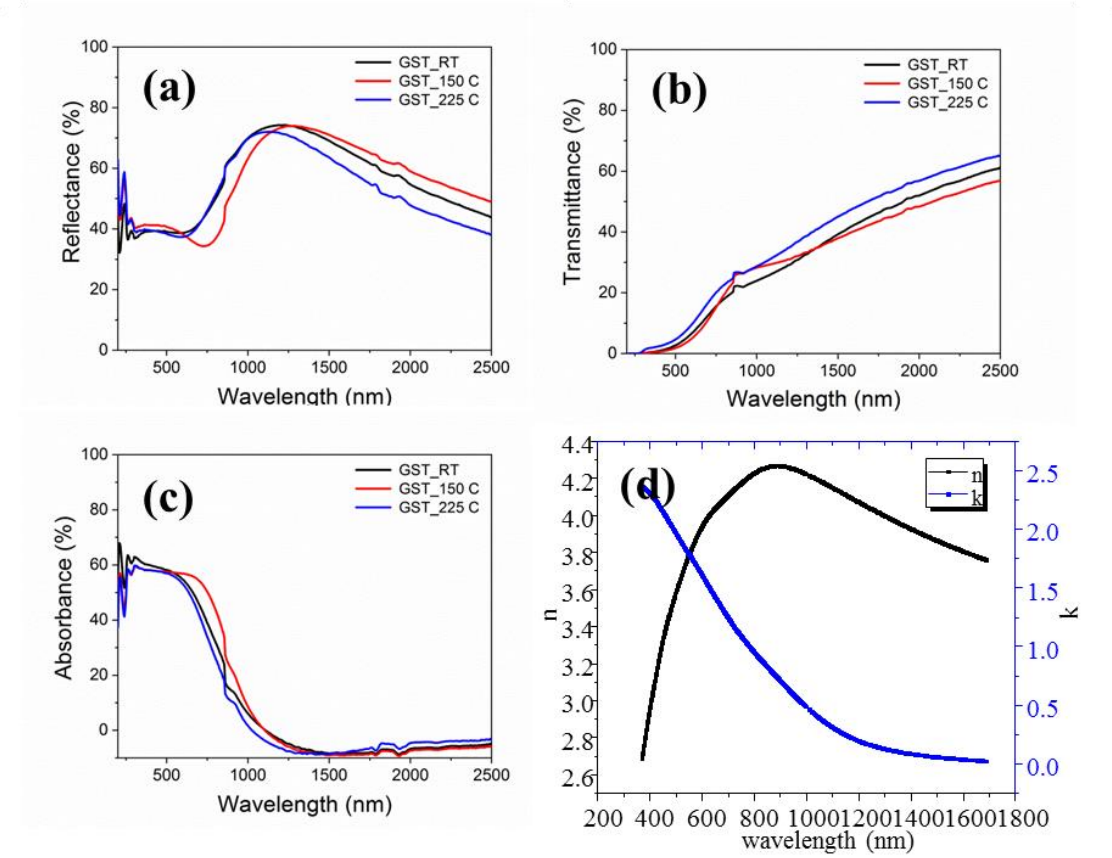

Figure 3.9 – (a) Reflection (b) Transmission (c) Absorption (d) Refractive index (n) and extinction coefficient (k) of GST films

(Image Credit: Dun Mao)

We tried analyzing the composition of GST by EDX (Energy-dispersive X-ray spectroscopy) as shown in Figure 3.10.a. The characteristic signatures of the elements

under consideration were: Ge having Kα - 9.8762 keV, Lα - 1.188 keV; Sb having Kα - 26.3595 keV, Lα - 3.6048 keV and Te having Kα - 27.4727 keV and Lα - 3.7694 keV. In order to detect Kα peak we started with an accelerating voltage of 30 kV. However, none of the peaks were detected. To detect the composition by finding Lα we reduced the accelerating voltage to 5 kV and the analysis graph is shown in Figure 3.10.a. The tool was only able to detect Ge and Si (from Substrate). The level of Sb and Te were below the noise level in the spectra due to which their relative ratio was not able to be determined. The EDX was probably not able to find the Ge, Sb and Te signatures because the penetration depth of the electron beam incident on the sample might be more than the thickness of the sample. In order to quantify the penetration depth of an electron beam we have performed Monte-Carlo simulation considering electron as a wave of wavelength (λ) given by

$$\lambda = \frac{h}{\sqrt{2meV}} = \sqrt{\frac{1.5}{V}}\ \text{nm}$$

where h - Planck's constant (6.626 x 10^{-34} J s), m - electron mass (9.109 x 10^{-31} kg), e - electronic charge (1.60 x 10^{-19} C), V - accelerating voltage (0.5 – 3 x 10^{4} V), V – accelerating voltage (wavelength of beam is controlled by accelerating voltage) and hence the penetration depth depends on V. We used the software CASINO - "monte CArlo SImulation of electroN trajectory in sOlids" for finding the penetration depth. The penetration depth of electron for 30 keV electron beam is about ~ 6 μm which explains why we were not able to detect any Kα peaks in the film at 30keV accelerating voltage. Whereas penetration depth of electron for 5 keV electron beam is about ~ 250 nm as can be seen in Figure 3.10.b. Therefore most of the backscattered

electron comes from the bulk of the device and to use EDX to detect atleast Lα peak we need sample of thickness more than 300 nm.

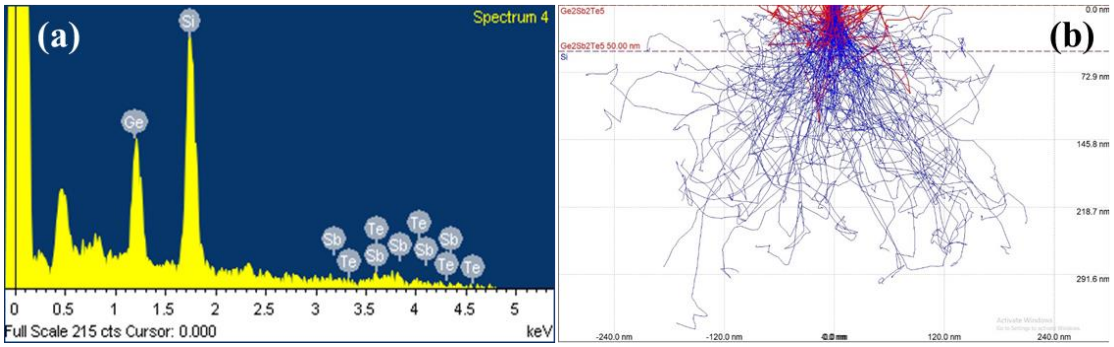

Figure 3.10 – (a) Energy-dispersive X-ray spectroscopy of GST film (b) Monte-Carlo simulation to find penetration depth of electron for 5 keV electron beam

The Raman spectra of the GST films at different temperatures are given in Figure 3.11.a. The spectra show 4 peaks namely - E mode of $GeTe_4$ tetrahedral at 80 cm^{-1}, $GeTe_{4-n}Ge_n$ (n=1,2) or Ge-Te peak at 125 cm^{-1}, A^2_{1g} mode of Sb_2Te_3 at 153 cm^{-1} and Ge-Ge units peak at 300 cm^{-1}. We find that Sb_2Te_3 peak is almost constant and doesn't vary with temperature whereas the Ge-Te peak initially increases when temperature increases to upto 150 °C and then decreases at 225 °C. Thus we consistently observe an anomalous behavior at 150 °C while measuring Raman, UV-VIS-NIR spectroscopy as well as AFM inspite of not showing any crystalline behavior in XRD. To better understand GST at 150 °C we did the Transmission Electron Microscopy (TEM) of the sample with reference to GST at RT. From Figure 3.11.b and c which shows the electron diffraction pattern, we observe that GST at RT is completely amorphous due to the concentric rings. This is because an amorphous material has short-range order and does not have any discrete reflection resulting in

diffraction along all directions resulting in diffuse ring patterns. On the other hand for GST at 150 °C, we find individual reflections within the rings. These individual reflections correspond to diffraction coming from the crystalline phase. Since there are multiple such individual reflections within the concentric rings it means there are crystals with different orientation meaning that there exists a polycrystalline phase for GST at 150 °C. This explains why the property of GST at 150 °C is different from GST_RT and GST_225 °C.

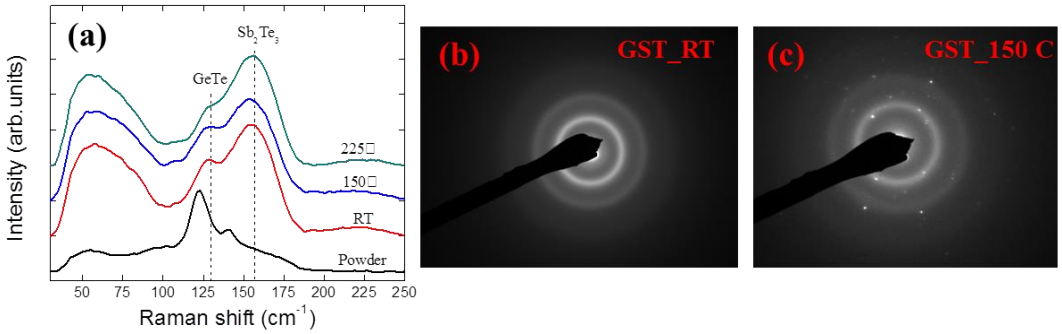

Figure 3.11 – (a) Raman spectra of GST films. Electron Diffraction pattern by TEM for (b) GST at RT (c) GST at 150 °C

The GST films we fabricated were then used for making waveguide structures using laser ablation by a pulsed laser. The micromachining of GST has been explored using lasers to create 2D and 3D photonic structures for future applications [13]. This could be of value to make cheaper photonic circuits without using e-beam lithography. High power Nd:YAG laser generating picosecond pulses were used for making laser inscriptions. Figure 3.12.a shows the optical image of the laser scribe made on GST by varying the power from 0.24W (37%) to 0.75W (40%). By optimizing the laser

condition we have gone down to feature size of 2 μm. From the SEM shown in Figure 3.12.b, we can see the crystallization of GST at the laser scribed region. We continue to optimize this parameter and apply it to devices in our future work.

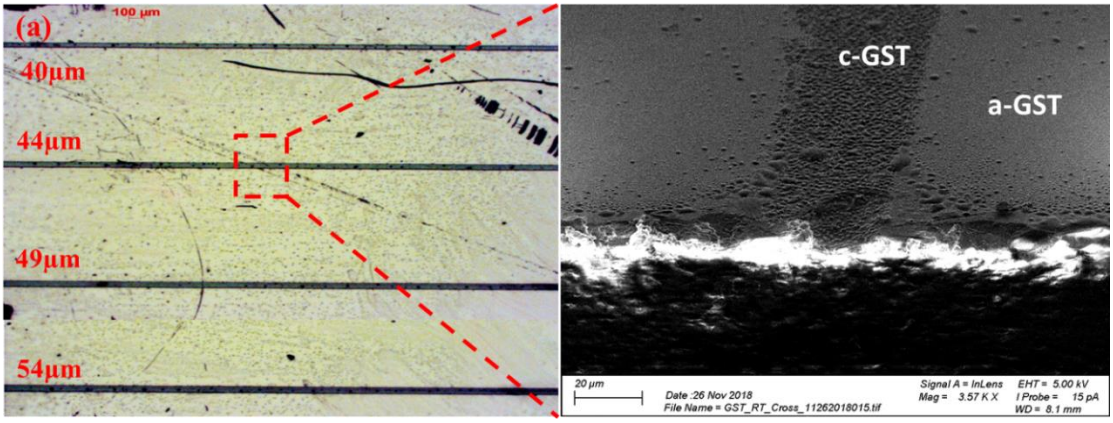

Figure 3.12 – (a) Optical image of laser scribed GST (b) Cross sectional SEM showing localized crystallization by laser inscription

(Image Credit: Dun Mao)

3.3 Graphene

Graphene is an allotrope of carbon in sp^2 hybridized state, having a honeycomb structure. It is one of the most well studied two dimensional (2D) material known for its semi-metallic properties having unique properties like high carrier mobility, high thermal conductivity, high Young's modulus, high transparency etc helping it find application in many photonic and electronic devices [14]. There are different methods by which we can get graphene for device level application, some of the include CVD, chemical exfoliation, mechanical exfoliation, liquid-phase ultrasonic exfoliation, exfoliation by micromechanical cleavage etc. Since Graphene has weak Van Der Waal's forces between the adjacent sheets exfoliation is considered as a feasible method to obtain single layer graphene[15,16].

In order to verify we have a monolayer of Graphene after the transfer process, we have used Micro-Raman Spectroscopy as an analysis tool. We have used 532 nm (green) laser Thermo Scientific DXR Micro- Raman Spectroscope for determining the Raman scattering from single layer Graphene. The incident power was kept as low as 0.1mW with a spot size of 0.7μm. It has a resolution of 1 cm^{-1} with a slit aperture width of 25 μm. We scan from 100 to 3500 cm^{-1} and the exposure time is set at 10 seconds with 3 scans to find the inelastic scattering peak of Graphene.

The spectra show 2 peaks at 520 cm^{-1} and 950 cm^{-1}, which originate from the 1^{st} and 2^{nd} order phonon scattering of the crystalline silicon substrate [17]. The graphene film shows a characteristic G peak at ~ 1580 cm^{-1} and a 2D peak at ~ 2700 cm^{-1} as observed in Figure 3.13 which is used to understand if the transferred Graphene is a monolayer. The Graphene films grown in this section were grown by thermal CVD during my summer internship at U.S. Army Research Lab under the guidance of Dr. Robert Burke. The G films were grown on 25-μm thick Cu foils without any pre-cleaning in a 1-inch hot wall tube furnace. The fused silica tube was loaded with Cu foil, then evacuated and filled with hydrogen. It was then heated to 1000°C and maintained at a chamber pressure of 40 mTorr under a 2 sccm H_2 flow. The Cu foil was stabilized at the desired temperatures of 1000°C. We then introduced 35 sccm of CH_4 for 10 minutes at a pressure of 500 mTorr. After exposure to CH_4, the furnace was cooled to room temperature.

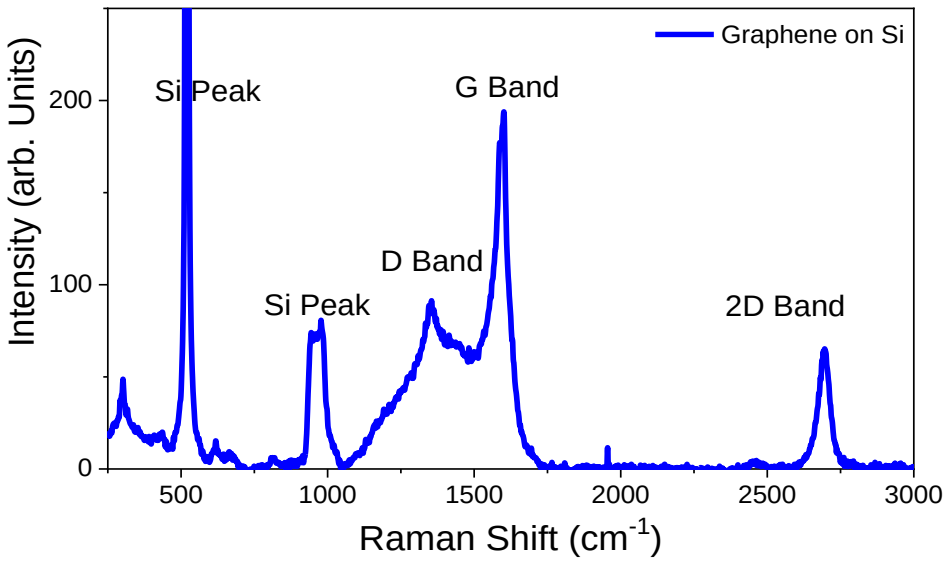

Figure 3.13 – Raman spectra of Graphene showing its characteristic peaks

Graphene (G) transfer is a delicate process which is sensitive to user handling since the process induces defects, folding of the monolayers resulting in poor transfer quality. The transfer recipe has been developed so that Graphene transfer can be locally done in our lab and we can put graphene over the photonic chips which we fabricate in the cleanroom. The first step involves cleaning all the substrates and the petri-dishes to be used for G transfer using Acetone, IPA and N_2 dry. Then mount the copper foil to a glass slide with G layer on top using Kapton tapes at the edges. Make sure the area coverage of the kapton over the Cu foil is minimal to utilize the entire G layer for transfer. Spin coat Poly (methyl methacrylate) (PMMA – 495 A6) at 4000 rpm for 1 minute to give an approximate thickness of 310 nm. Bake it at 170 °C for 2 minutes. Repeat this procedure thrice to get a total thickness of ~930 nm thick

PMMA. Then remove the kapton tape from the edges, carefully flip the Cu foil and tape the edges again using kapton to prepare the sample for plasma ashing. The rear side of the Cu foil is now subjected to a descum recipe in the plasma asher to remove any residual G on the rear side formed during CVD. The asher which is nothing but an oxygen plasma maintained at 320 W at a pressure of 1.3 Torr with an O_2 flow rate of 1000 sccm for 10 minutes helps oxidize any residual G on the back side which will prevent the etching of the Cu foil. After ashing, gently immerse the Cu foil with G on top into Ferric chloride solution ($FeCl_3$) such that the foil floats on the solution. We slowly find the Cu foil being etched away and the G layer afloat on the solution supported by PMMA. We then scoop the fragile PMMA/G using a glass slide and immerse it into DI water followed by transfer into HCl (Hydrochloric acid) to remove any iron contaminants. It is again scooped and transferred to DI water from where it is transferred onto the actual chip. We then air dry the sample for ~10 minutes and bake it in the oven for ~ 30 minutes at 45 °C. This is followed by a hot plate step at 170 °C for ~5 minutes to harden the PMMA (PMMA has a glass transition temperature at ~150 °C). We then rinse the sample in acetone/IPA to remove the PMMA resist to give only G on top of the chip.

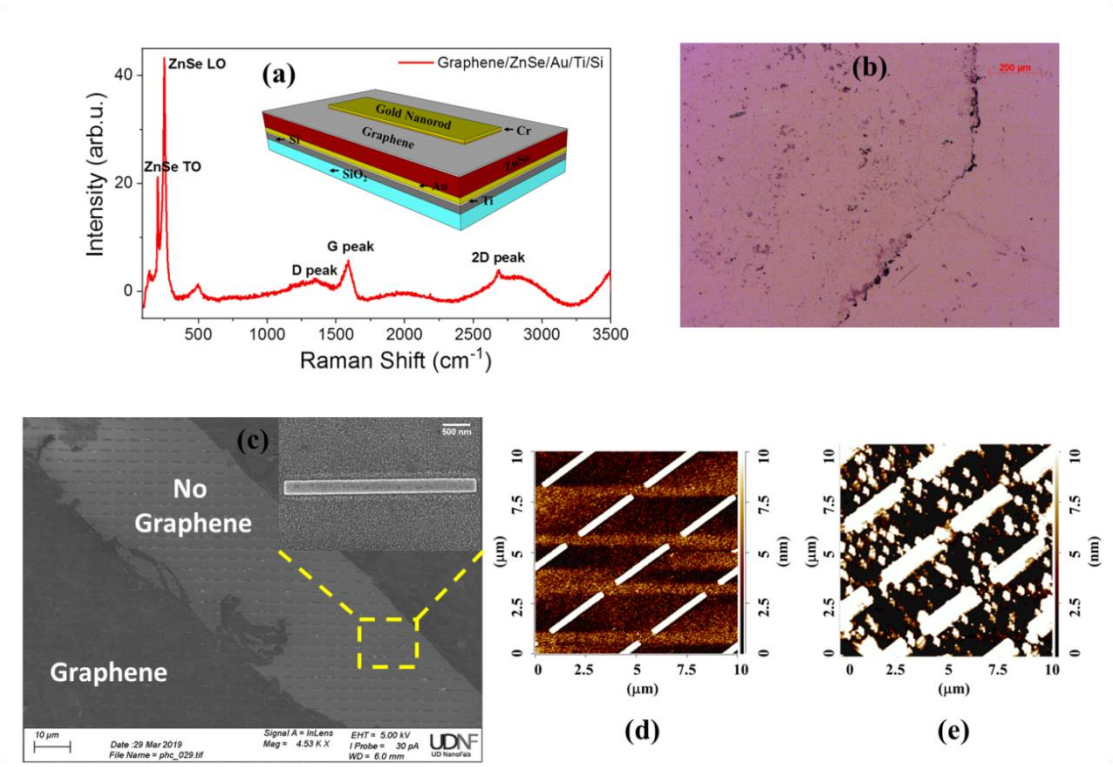

Figure 3.14 – (a) Raman spectra of the Graphene on ZnSe and the device structure (b) Graphene transferred to ZnSe (c) SEM of Nanorods showing Graphene and No Graphene region (Inset: Single Nanorod). AFM of (d) Nanorod without Graphene (e) Nanorod with Graphene

(Image Credit: Thomas Kananen)

After successfully developing the method for transferring G we have applied it to some device architectures. In Figure 3.14.a we can see a device structure involving gold nanorod array which is used for gas detection [18]. The Raman spectra gives the peak for G as well as ZnSe. Figure 3.14.b shows the G transferred onto ZnSe substrate which acts as a spacer. Figure 3.14.c shows the region with and without G coverage. Similarly, Figure 3.14.d and e gives the AFM image of the nanorod structure with and without Graphene. The details of the characterization of these devices as well as it

working will be explained in our future work. Some of the other applications of our G transfer has been reported elsewhere [19].

3.4 Indium Selenide (In_2Se_3)

Indium Selenide (InSe) is a semiconductor chalcogenide which is known for its direct bandgap [20] (~1.25 eV at room temperature), chemical stability and its phase changing properties. InSe is a III-VI chalcogenide which has been less explored in photonics and recently InSe flakes has found application in photodetectors due to its high responsivity and quantum efficiency [21]. In this work, we have grown ~50 nm thin films of InSe using Molecular Beam Epitaxy (MBE) growth method using the MBE system from Dr. Stephanie Law's group in the Material science department and later mechanically exfoliated to be applied for photonic chips. The exfoliation process has been explained in detail this section and its application in photonic circuits will be shown in our future work.

There are different methods to mechanically exfoliate materials; in this study, we have used thermal release tapes. PDMS (10:1) solution is also used for exfoliation of In_2Se_3 on Sapphire (Al_2O_3) substrates deposited by MBE however the focus of this work is only using thermal release tapes and the exfoliation method is described below.

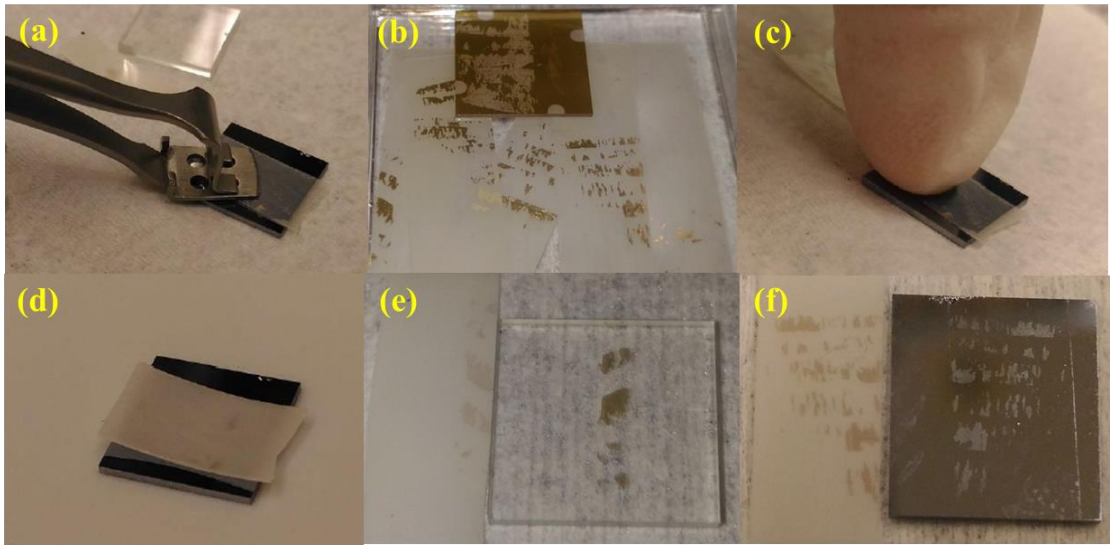

Figure 3.15 – (a) Flattening of tape using tweezer (b) Peeling of InSe from substrate using release tape (c) pressing the release tape on the substrate to be transferred (d) Peeling of release tape at higher temperature (e) InSe flake transferred to glass (f) InSe flake transferred to silicon

- ***Substrate (Glass/Silicon) cleaning for Transfer***

Sonicate substrate in acetone and IPA (Iso-Propyl Alcohol) for 3 minutes each followed by nitrogen drying the sample. For critical samples requiring minimal contaminants, an additional cleaning step includes plasma ashing the sample for 10 minutes and cleaning using Nano-Strip (sulfuric acid and hydrogen peroxide mixture).

- ***Pre-baking***

Keep the substrate on to which the film has to be transferred, in hot plate (150℃) for 5 minutes to remove any moisture condensed on the surface of the sample before the transfer of In_2Se_3.

- ***Transfer Process***

Remove the sample from the hot plate and keep it aside to reach room temperature. Meanwhile, stick the thermal release tape (white and translucent) on the surface of the In_2Se_3 sample grown by MBE. (Ideally, stick from one end to another to avoid bubble formation). With the edge of the tweezer, slide from one end to another to remove any air bubbles. Flatten the tape using tweezers such that the tape completely sticks to the In_2Se_3 substrate as shown in Figure 3.15.a. Quickly peel off the thermal release tape to get large flakes of In_2Se_3 as shown in Figure 3.15.b. Stick the peeled off thermal tape with InSe flakes on to the cooled substrate. Again, with the edge of the tweezer slide from one end to another to remove any air bubbles as shown below: (A Q tip can also be used to be more delicate incase if the user is not familiar with using tweezers delicately without causing scratches). Press the tape on the sample for 2 minutes after removing the air bubbles as shown in Figure 3.15.c. Meanwhile, let the hot plate be set at 110℃ and be stabilized. Once it is stabilized at 110℃, place the substrate with the thermal release tape onto the hot plate. The thermal tape will be automatically peeled off as shown in Figure 3.15.d completing the transfer process. The InSe flakes transferred on glass and silicon are shown in Figure 3.15.e and 3.15.f respectively.

The optical image of the InSe flake transferred on glass and silicon are shown in Figure 3.16.a and 3.16.c respectively. We find that each flake which spans hundreds of microns actually consists of smaller flakes of the order of 2-50 μm as can be seen in the magnified Figure 3.16.b and 3.16.c respectively. Thus we observe that though flakes of the order of millimeters are transferred on the substrate the actual continuous films are only of the order of 2-50 micrometer as can be observed in the zoomed

images. The coverage area of the flakes is better for glass as compared to silicon. The transferred flakes are characterized by micro-Raman spectroscopy as can be seen in Figure 3.16.e. The spectrum shows a sharp peak at ~ 110 cm^{-1} implying that the InSe is in β-phase after MBE growth. The application of these flakes for photonic structures will be shown in our future work.

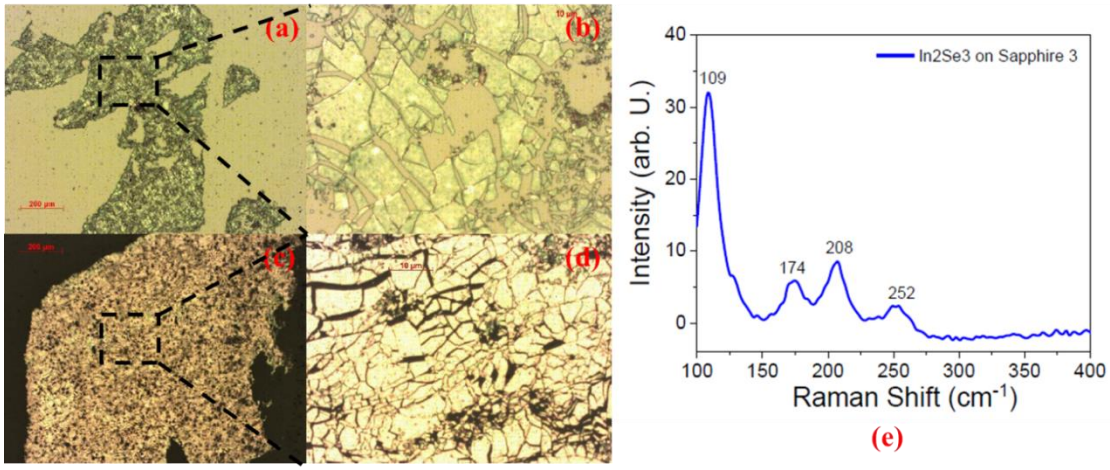

Figure 3.16 – (a-b) InSe flake transferred on silicon (c-d) InSe flake transferred on glass (e) Raman spectra of InSe grown on sapphire by MBE which was transferred to silicon by exfoliation

3.5 Organic Materials

In this section, we have explored organic materials which can find application in photonic circuits. Though materials like poly(3,4-ethylene-dioxythiophene): polystyrene sulfonate (PEDOT: PSS) have been used extensively as electrode material in devices we have investigated some new organic materials which can find potential application in photonics. One of the first parameters we would like to know is the resistance of these materials to find application in electronic or photonic circuits. In this work, we have investigated methods to find the resistivity of one such novel

polymer material. In this work, we have used an ionomer like Poly (Aryl Piperidinium) developed by Dr. Yushan Yan's Group which has an alkaline-stable cation, piperidinium, introduced into a rigid aromatic polymer backbone free of ether bonds. It has properties like superior chemical stability, hydrophilic nature, hydroxide conductivity, decreased water uptake, good solubility in selected solvents, improved mechanical properties in an ambient dry state and is stable with most metals (non-reactive) – so we could select any metal for electrode (in our work we have used Au/Cr – for better adhesion).

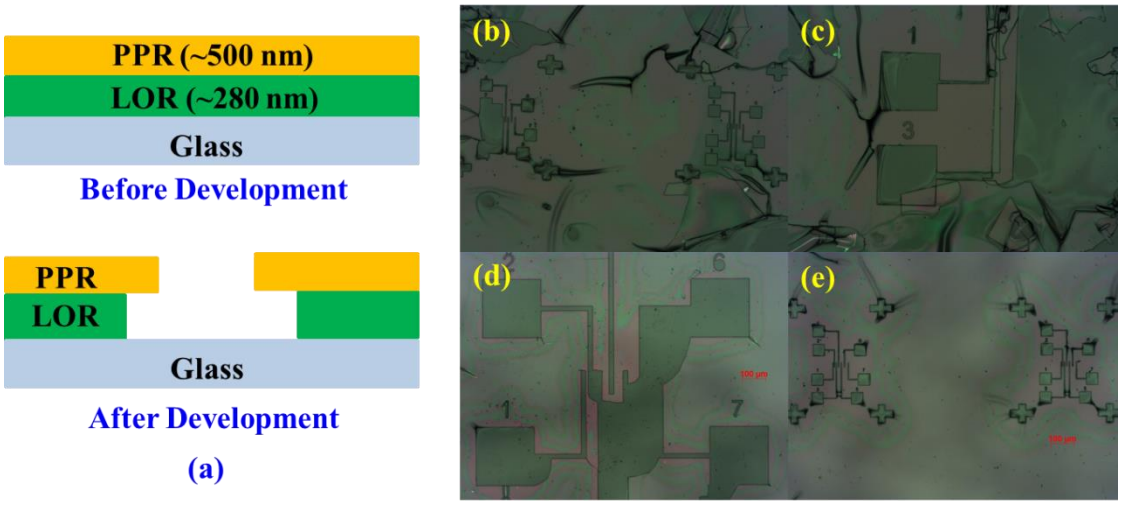

Figure 3. 17 – (a) Schematic of development of 2-layer resist for electrode deposition. (b-c) Overdevelopment of resist (d-e) Adhesion issue of the resist

The steps for fabrication of Transmission Line Measurement (TLM) structures to measure contact resistance are given below (2 inch^2 glass sample): We start with organic cleaning (sonication in acetone/IPA and N_2 drying the sample). We then spin coat it with lift-off resist (LOR 3A) at 2000 rpm for 60 seconds to get a thickness of ~280 nm. We then bake the sample at 200 °C for 5 minutes. The sample is then spin-

coated with a 2nd layer of positive photo resist (PPR) called AZ 701 MIR 11CP (AZ MIF 701) at 4000 rpm for 60 seconds (~500 nm). It is then baked at 90 °C for 90 seconds. At this stage, the 2 step resist looks like the schematic shown in Figure 3.17.a. The electrode pattern is then transferred by laser writing at a dosage of 480 mJ/cm^2. It is then followed by a post bake at 110 °C for 90 seconds. The pattern is developed with MIF 300K for 60 seconds then DI water rinsed for ~30 seconds and N_2 dried. The development process is very critical and care has to be taken to prevent over or under development. Initially while optimizing, we developed for 75 seconds which resulted in the sample to be over developed as can be observed in Figure 3.17.b and c. The LOR completely dissolved in the developer solution resulting in PPR design to float. After development, we see the resist has been removed from the electrode region where we will deposit the metal as shown in Figure 3.17.a. Please note the undercut of LOR which will facilitate lift-off. It is also important to note that while using glass substrate there can also be an adhesion issue of the LOR which will result in poor pattern transfer as can be seen in Figure 3.17.d and e. To overcome this issue, we tried both ways of surface priming previously discussed in section 2.1. We did HMDS Treatment (10 minutes) for adhesion promotion of SiO_2 surface (Glass). However, we found the spin coating of adhesion promoter (AR-300-80) gave better pattern transfer due to improved adhesion.

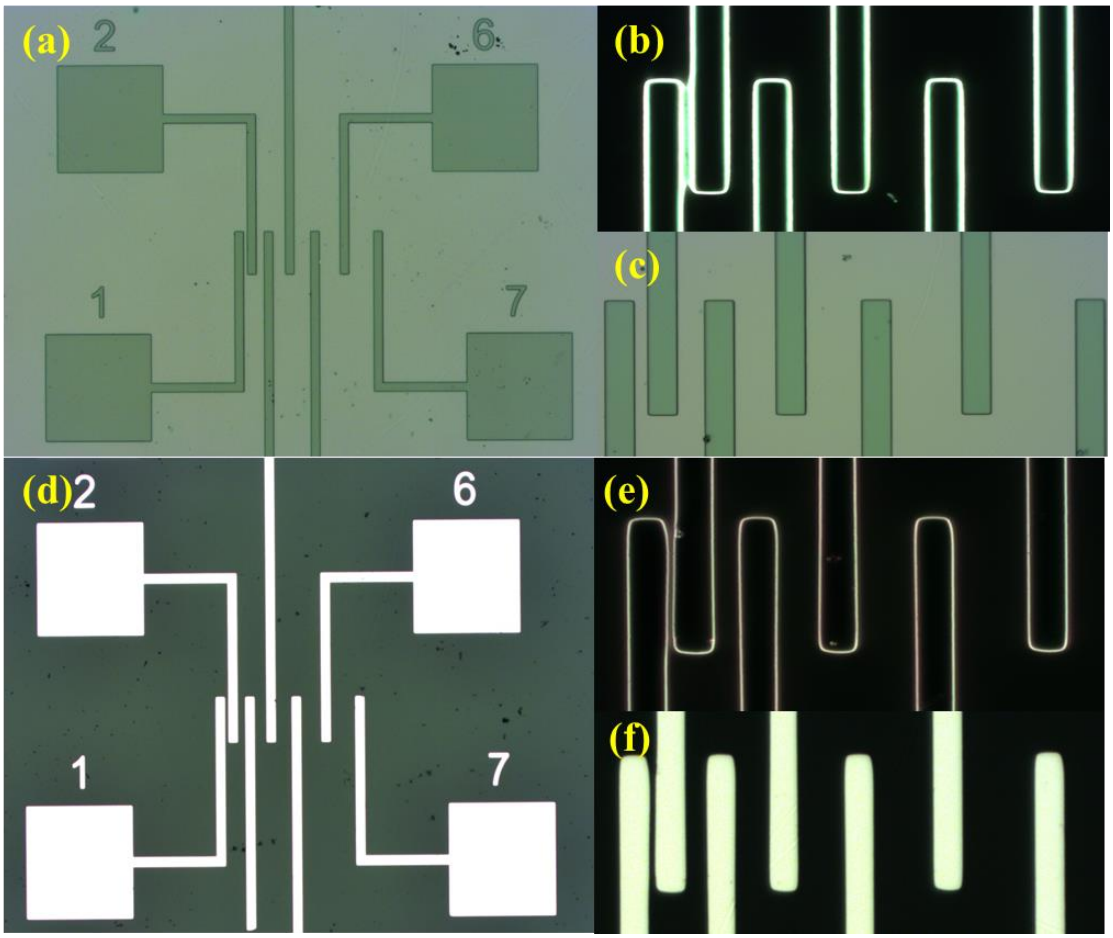

Figure 3.18 – (a) Pattern transfer after development (b) Dark field (c) Bright field image of the TLM structure after development (d) Pattern transfer after metallization (e) Dark field (f) Bright field image of the TLM structure after metallization

This can be verified from Figure 3.18.a. The dark and bright field optical image as shown in Figure 3.18.b and c shows good pattern transfer with no over or under-developed regions. We then deposit the electrode metal i.e. 10 nm (Cr) + 100 nm (Au) by electron-beam evaporation. Lift off process was then done by NMP (at 45°C) for ~ 10 minutes with intermittent ultra-sonication. After lift off the metalized electrode can be seen in Figure 3.18.d. Similar to the previous step the dark and bright

field optical images in Figure 3.18.e and f shows the metal electrode design has been realized successfully. After metallization and we put the polymer onto the TLM structures by dropping the polymer with I- anion onto the active region with fiber tip under a microscope. We then baked it in the oven at 50 °C for 15 minutes and performed the I-V test of the structures.

The SEM image in Figure 3.19.a shows the spacing between the electrodes and Figure 3.19.b shows the polymer drop casted over the TLM electrode for I-V measurement. We performed the I-V with the increasing electrode distance to find contact resistance. We observed that for the electrode which has the least distance between them the I-V curve is exponential as can be observed in Figure 3.19.c whereas as the distance increases the I-V curve tends to have a linear relationship as seen in Figure 3.19.d. We found the initial exponential behavior of the I-V curve due to the degrading electrode caused by leaching of I^- ions from the polymer which raises concern of the stability of the polymer in electronic circuits. From the I-V measurements, we calculated the polymer-gold contact resistance to be 2.7×10^9 Ω and sheet resistance to be 4×10^9 Ω. The resistivity of the polymer (assuming the thickness of the polymer is 5 micrometer) was found to be 2×10^4 Ω.m. We plan to further study this material for its stability and apply in actual devices with novel architectures in the future.

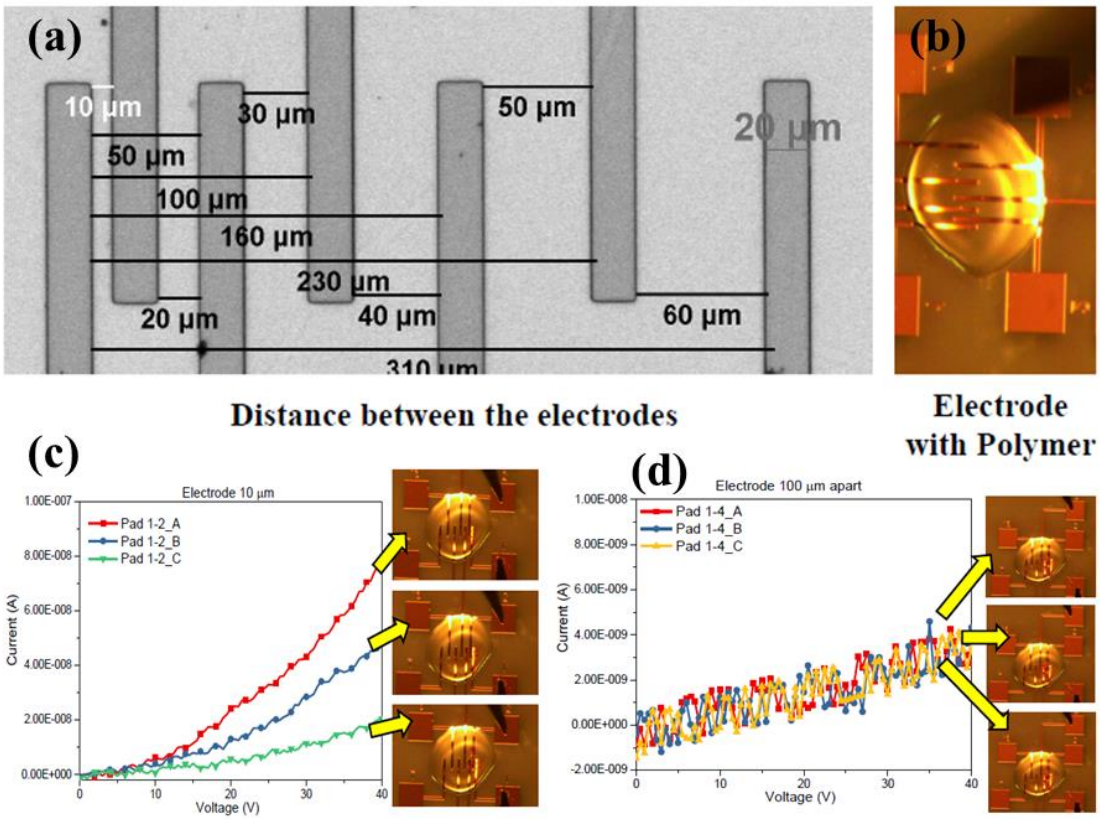

Figure 3.19 (a) SEM of TLM structure showing electrode spacing. (b) Polymer drop casted on electrode (c) I-V between electrode 1-2 (d) I-V between electrode 1-4.

Chapter 4

CONCLUSION

4.1 Summary of Results

In this thesis, we have developed fabrication process flow for different passive and active photonic device components like waveguides, diffraction grating couplers, micro-ring resonators and photonic crystal waveguides. The challenges involved in the fabrication process, as well as the solutions for these problems, are discussed. The process steps have been optimized based on these bottlenecks. This fabrication optimization can act as a reference guideline for making advanced structures with the same concepts. We have developed a wide variety of materials which can find application in photonics. Along with structures on silicon on insulator (SOI) we have also considered the possibility of using amorphous silicon as the core material. The initial work for amorphous silicon photonics has been established which can be further optimized for making low loss and functional photonic devices. We have performed a detailed characterization of bulk chalcogenide like GST to be used as a cladding layer in photonic circuits. Exfoliation methods of chalcogenides like InSe have been developed which can be used for photonic devices. G transfer process has been developed for locally transferring G over photonic chips for multiple applications. We have also explored the possibility of using organic material in photonics.

4.2 Future Work

In the future, we wish to further optimize the fabrication to obtain low loss waveguides and couplers with no breakage or defects. Advanced concepts to understand the physics of micro-ring resonators will be explored and the effect of GST

cladding layer or intentional scattering element like a notch will be explored. We wish to further develop photonic crystal waveguides with lower loss and use 2D materials over it to use it as photodetectors. Amorphous photonics can be a viable method to make low loss photonic circuits due to their lower cost and industrial feasibility, so we will continue to make low loss amorphous silicon photonic devices. GST will be used for micromachining by laser as well as cladding layer to other photonic circuits. Exfoliated InSe can be used as an active material for modulators. The transfer process developed for G can help finding its application is different device architectures as photodetectors, modulators, sensors, electrode etc. We will study for the stability of organic material and find applications where they could be used as the gate material.

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