DESIGN, FABRICATION, ITERATION, AND TESTING OF THE 68X68 SUPERLATTICE LED INFRARED PROJECTION SYSTEM AND ASSOCIATED ELECTRONICS

by

Rodney Thomas Tyler McGee

A thesis submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Masters of Science in Electrical and Computer Engineering

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Approved: _____
Fouad E Kiamilev, Ph.D.
Professor in charge of thesis on behalf of the Advisory Committee

Approved: _____
Kenneth E. Barner, Ph.D.
Chairman of the Department of Electrical and Computer Engineering

Approved: _____
Michael J. Chajes, Ph.D
Dean of the College of Engineering

Approved: _____
Debra Hess Norris, M.S.
Vice Provost for Graduate and Professional Education

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ABSTRACT

Optoelectronic devices that emit in the mid-wave infrared (MWIR) and long-wave infrared (LWIR) wavelengths have traditionally targeted the 3-4 and 8-12 micrometer wavelength, because atmospheric absorption is minimal in the these windows. Infrared (IR) radiation has long been of scientific interest because the unique signatures of light emitted or absorbed can be remotely detected and characterized for all manner of objects and processes. Large IR detector arrays, particularly ones intended for military and/or aerospace applications, are often difficult and expensive to directly test. Ultimately for these detectors, an IR projector for scene simulation is required.

This thesis documents the creation and testing of a cryogenic integrated infrared projection system combining large two-dimensional arrays of superlattice light-emitting diodes (SLEDs) with a custom driver IC and FPGA-based control system. It covers a range of disciplines, design decisions, systems engineering issues, and personal observations on the process of the design, fabrication, iteration, and testing of the 68x68 SLEDs system. Several testing sessions showed the unique functionality and capabilities in several important areas such as: apparent temperature exceeding 1000 Kelvin, rise and fall time of a few microseconds, and over 90 percent functional yield. The work described in this paper provides the foundation for the 512x512 SLEDs system currently in development.

Chapter 1

INTRODUCTION

1.1 Backround

Optoelectronic devices that emit in the mid-wave infrared (MWIR) and long-wave infrared (LWIR) wavelengths have traditionally targeted the 3-4 and 8-12 micrometer wavelength because atmospheric absorption is minimal in the these windows [4]. Infrared (IR) radiation has long been of scientific interest because the unique signatures of light emitted or absorbed can be remotely detected and characterized for all manner of objects and processes. For example, in the infrared one can see the difference between grass that needs watering and heathy grass long before the green hue has changed. In another case, because of the light absorption of sugar one can tell the difference between water with dissolved sugar and plain water. Large IR detector arrays, particularly ones intended for military and aerospace applications, are often difficult and expensive to directly test, so for these detectors, an IR projector for scene simulation is required. The simulations are for various types of missile defense, tactical missile seekers, and other IR scenes used in the hardware in the loop (HWIL) sensor testing. The sensor testing requires large 2D array, high frame rate, high apparent temperature, and large dynamic range IR sources.

This thesis documents the creation and testing of a cryogenic integrated infrared projection system combining large two-dimensional arrays of superlattice light-emitting diodes (SLEDs) with a custom driver IC and FPGA-based control system. It covers a range of disciplines, design decisions, systems engineering issues,

and personal observations on the process of the design, fabrication, iteration, and testing of the 68x68 SLEDs system. Several testing sessions showed the unique functionality and capabilities in several important areas such as: apparent temperature exceeding 1000 Kelvin, rise and fall time of a few microseconds, and over 90 percent functional yield. The work described in this paper provides the foundation for the 512x512 SLEDs system currently in development.

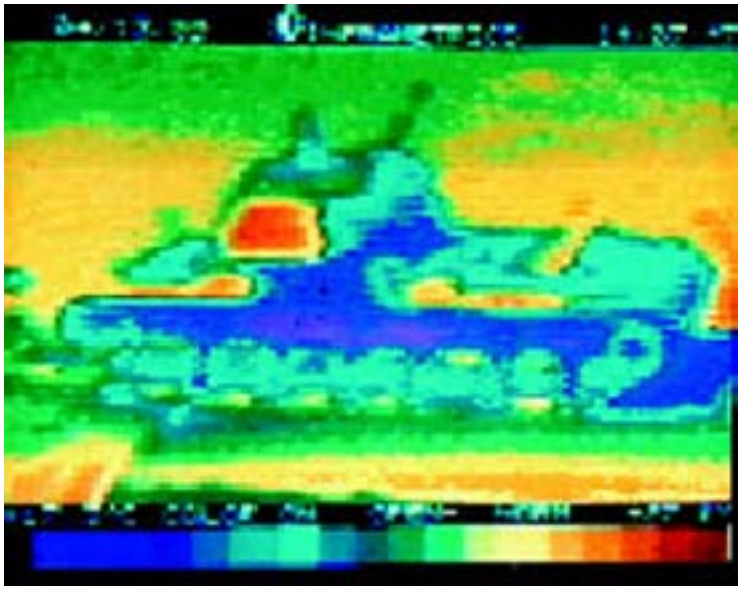
1.2 Motivation

The University of Iowa created devices capable of emitting the infrared; however they lacked the large scale electronically controllable driver array and the associated electronics. CVORG, a research group at the University of Delaware, was initially challenged to design and fabricate an integrated circuit (IC) that implemented a high-power parallel light emitting diode (LED) driver. The unique features about this design were the large number of channels (4,624) and high current drive capability (100mA). The design was organized similarly to a analog DRAM. The driver is laid out like two dimensional array where each cell or pixel has an analog memory in the form of a capacitor that holds the value of each pixel for a few milliseconds. A simplistic row/column selection method is used to address each pixel; however, the number of pins required to operate every row and column independently is a drawback.

Other driver chips with similar channel counts typically can drive at most a few milliamps. Functionally, the chip is organized like an analog DRAM – it contains a two-dimensional array of LED driver cells. Each driver cell has an analog memory that remembers the last value written to it for several milliseconds. A simple row/column selection scheme is used to select the driver cell in the array. Once selected, the driver cell receives and stores an analog input voltage. This input voltage is converted by the cell to LED drive current. By continuously and sequentially rewriting the entire array at KHz rates, the array can be made to drive parallel

LED arrays. The circuit design replicates a single NPN bipolar and CMOS LED driver cell to achieve high-current operation and analog memory storage. Careful attention is paid to signal and power routing using all 7 metal routing layers. The design and fabrication of the SLEDs read-in integrated circuit (RIIC) was originally an exercise in engineering and design; however, this was only the beginning of a longterm multigenerational research project.

Figure 1.1: Infrared image of a tank recorded with the 3-5micron infrared imaging camera [1]



1.3 Related Work

Several IR source technologies have been integrated into the HWIL systems in the past, including a scanning laser array, resistive array, and digital micro mirror devices. The state of the art resistive array projector systems have limited frame rate capability due to the transition associated with the resistors. Resistor array technology is limited to an apparent temperature less 800 Kelvin and rise times around 5 milliseconds. Scanning laser projectors have other issues like a smearing effect

and non-uniformity [5]. Optical modulator based projectors (digital micro mirror) produce an insufficient extinction ratio. Mid-wave infrared (MWIR) light emitting devices (LED) offer an attractive alternative for IR scene projection. MWIR LEDs are desirable for IR scene projection because of considerable advantages in terms of cost, volume, long term reliability, and fast switching speed.

Chapter 2

HIGH POWER PARALLEL LED DRIVER

2.1 Purpose

The driver chip controls the activation and intensity of the SLEDs, and when interfaced with a FPGA the driver chip can draw patterns and arbitrary shapes by utilizing the control lines.

2.2 Specifications

The initial circuit design work for the driver chip was done by Jeremy Ekman and Josh Kramer of CVORG. The die was fabricated on multi-project wafer run sponsored by DARPA and fabricated by IBM Microelectronics. The chip is designed in IBM 0.13 micron SIGE 8HP technology. The normal supply voltage is 2.7V. The deadline for submitting the completed design to the foundry broker May 8, 2006. IBM 8HP 200GHz 130nm technology was developed for 40Gbps telecom. This technology is not ideal for LED drivers; however, it does have seven layers of metal instead of the typical three or four. Also, the copper interconnect current density is 5mA/mm^2, as opposed to a more typical 1mA/mm^2 value. The NPN current capacity is 12mA/mm^2 instead of 1.2mA/mm^2 for a typical NPN and 0.07mA/mm^2 for a conventional 0.25mm CMOS process [6]. In 200GHz SiGe, it is possible to build a multi-channel driver with total current capacity of several amperes.

Figure 2.1: Unit cell schematic

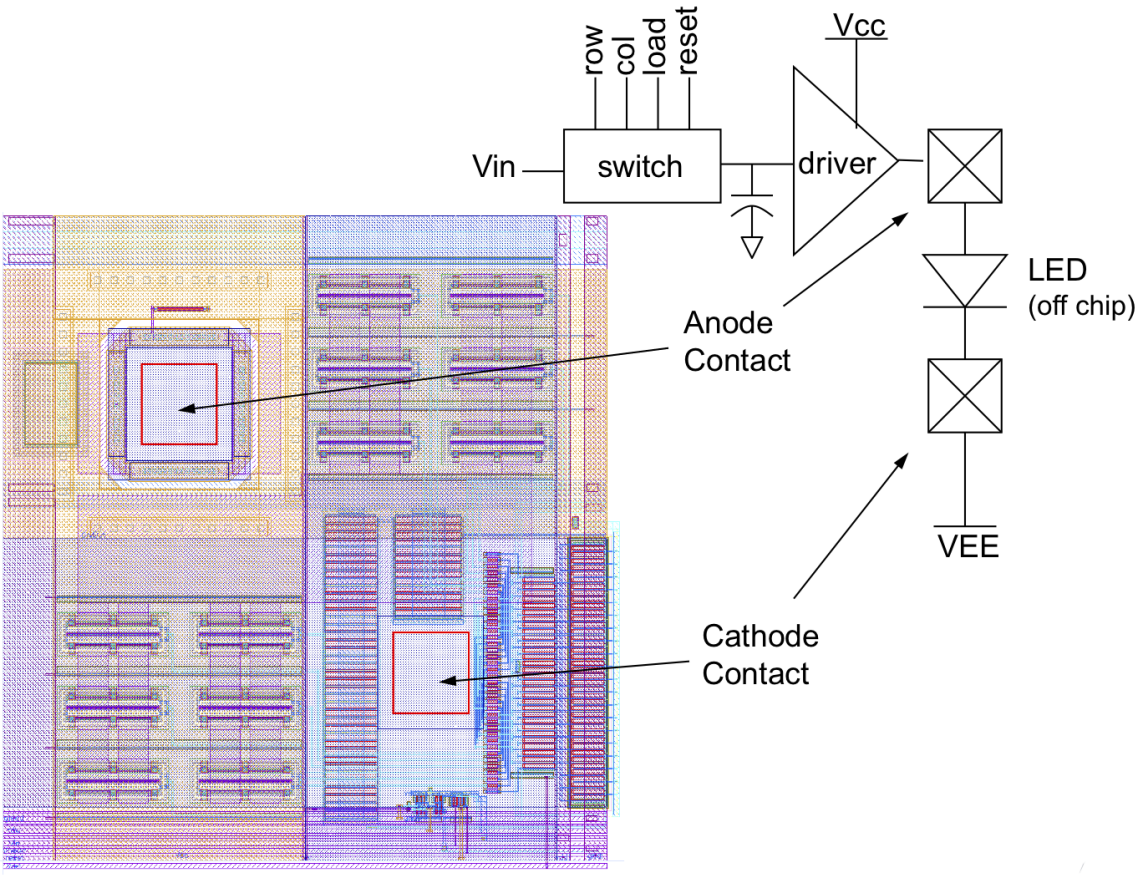


Table 2.1: Summary of specifications

Drive up to 68x68 sized LED arrays
Up to 4,624 individual LED devices
Designed for common cathode LEDs
Up to 100mA of direct drive current
Can accommodate LED devices with up to 8V voltage
10mm x 10mm bare die
10% of the array (400 LEDs) can be simultaneously driven
120 micron x 120 micron LED driver cell
ESD protection on all inputs
Uses simple parallel row/column addressing scheme
Low distortion analog voltage-to-current conversion
Designed for KHz refresh rate
Four corner driver cells implement special testability feature
Adjustable LED power supply voltage
Logic normal power supply of 2.5 volts
130 nanometer IBM 8HP SiGE Technology

2.2.1 Driver Perimeter Pads

The perimeter pads are the connections to the driver chip. Typically, the pads are connected to the chip carrier using small gold bond wires. Alternatively, temporary electrical connections for short term testing can be made using a probe station. The pads for this chip are shown in Figure 2.2

2.2.2 Verification of Driver Functionality

The initial testing of this device was to evaluate functionality of the SLED driver. An excessively large PCB was fabricated in order to control every digital control line on the chip – unfortunately was done by individually moving jumpers by hand. The chip was not electronically controllable. Therefore, each configuration was slow to change and transient responses to input were not easily obtainable. Since only the corners were testable in a driver-only configuration without the use of a probe station, the usefulness of controlling all columns and rows by hand was

Table 2.2: Driver perimeter pads

Name	Quantity	Type	Purpose
Vin	1	Analog	LED drive value
Gload	1	Digital	Loads Vin value into latches
Row Select	68	Digital	Select one or more rows
Column Select	68	Digital	Select one or more column
Reset	1	Digital	Input global reset of all latches
Reset Value	1	Analog	Input for reset value latches
Ibias	1	Analog	Current for bias control input
Vcc	68	Power	LED positive supply
Vee	68	Power	LED negative supply
Vdd	5	Power	Digital voltage supply
Gnd	6	Power	Digital voltage ground
Test Out	4	Test	Analog outputs connected to 4 corner drivers
Test In	4	Test	Analog inputs connected to 4 corner LEDs

Figure 2.2: LED driver in a CPGA package

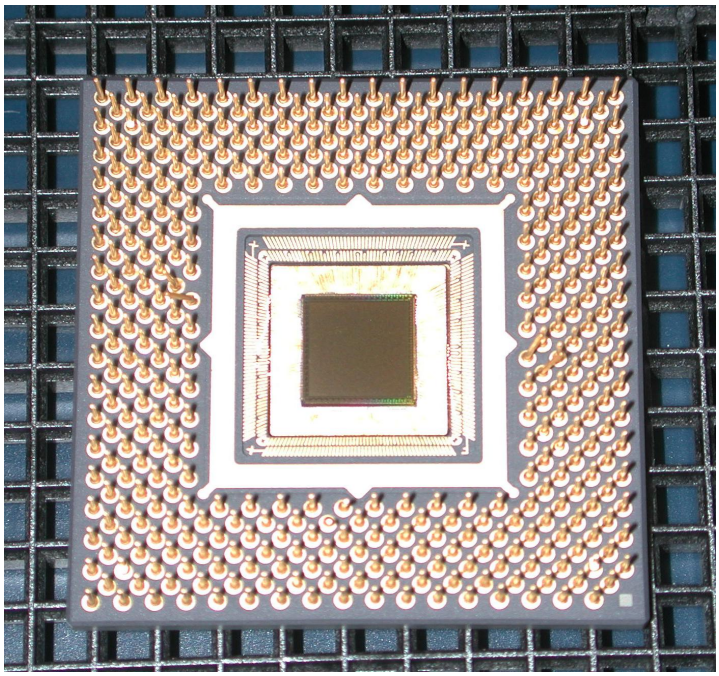
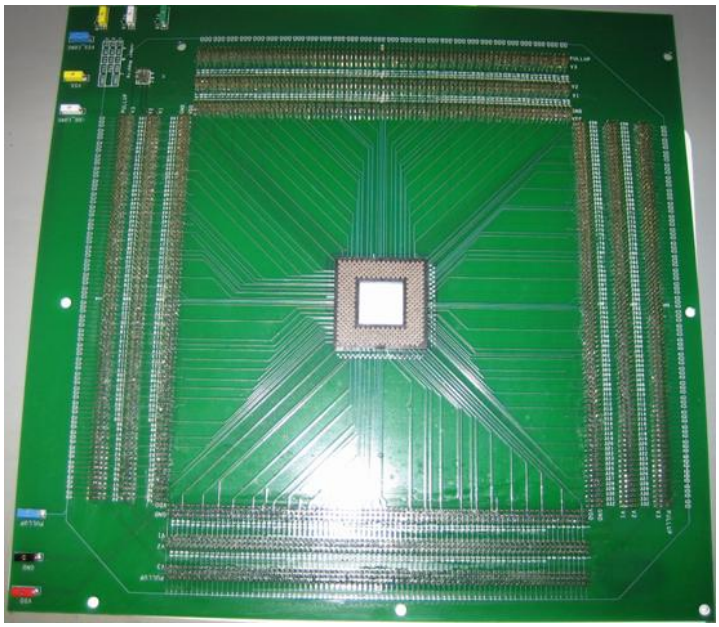


Figure 2.3: Giant PCB that holds CPGA package



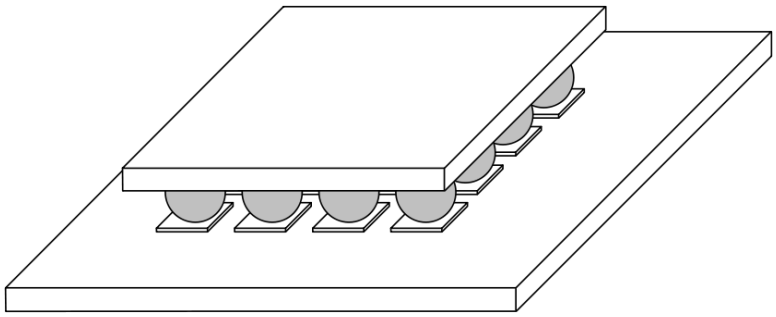
questionable; however there was a hole in the bottom of the PCB to allow optical testing of drivers with SLEDs attached. Testing with this board proved impractical and unsuccessful.

From a system engineering perspective, the use of this first generation driver chip in actual complete infrared projection system was slowed by the number of entities involved with integrating, hybridizing, and designing the test platform. The program was restructured later, making our research group responsible for everything except for the SLED devices. Our responsibility included the 68x68 driver RIIC, packaging, wire bonding, cryogenic cooling, interfacing PCBs and power electronics, digital/analog interface hardware, software control system, associated test equipment, and single element optical detection.

2.2.3 Hybridization

Flip-chip bonding is a process for interconnecting semiconductor devices with solder bumps which have been deposited onto the chip pads. The solder bumps can be deposited on the chip pads on the top side of the wafer during the final wafer processing step, or the solder bumps can be added the chips of a already diced wafer. During the mounting, the chip is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the other. This is combined with wire-bonding to connect the combined chip to external circuitry (see Section 3.2). For this project, this is how the SLEDs chip is attached to the driver chip and interfaced with the outside world. Each unit cell has two contact pads consisting of an opening in the final passivation to expose top-level metal on the ASIC. One contact is for the SLED anode (unique to each pixel) and one for the SLED cathode (common among the entire array).

Figure 2.4: Example of flip chip with bumps [2]



2.3 Apparent Temperature

A black body is an ideal object because it absorbs electromagnetic radiation. In addition, no electromagnetic radiation passes through or is reflected by a black body. Because no visible light is reflected or transmitted, the object appears

Figure 2.5: Anode contact structure

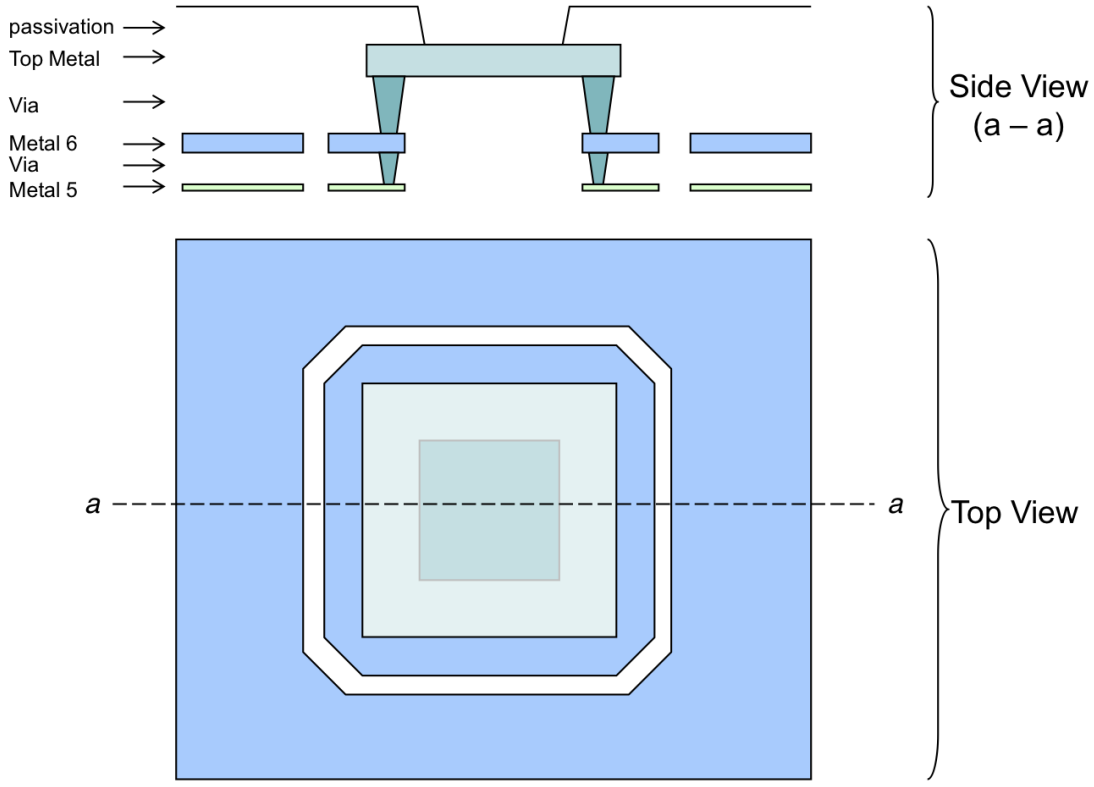


Figure 2.6: Cathode contact structure

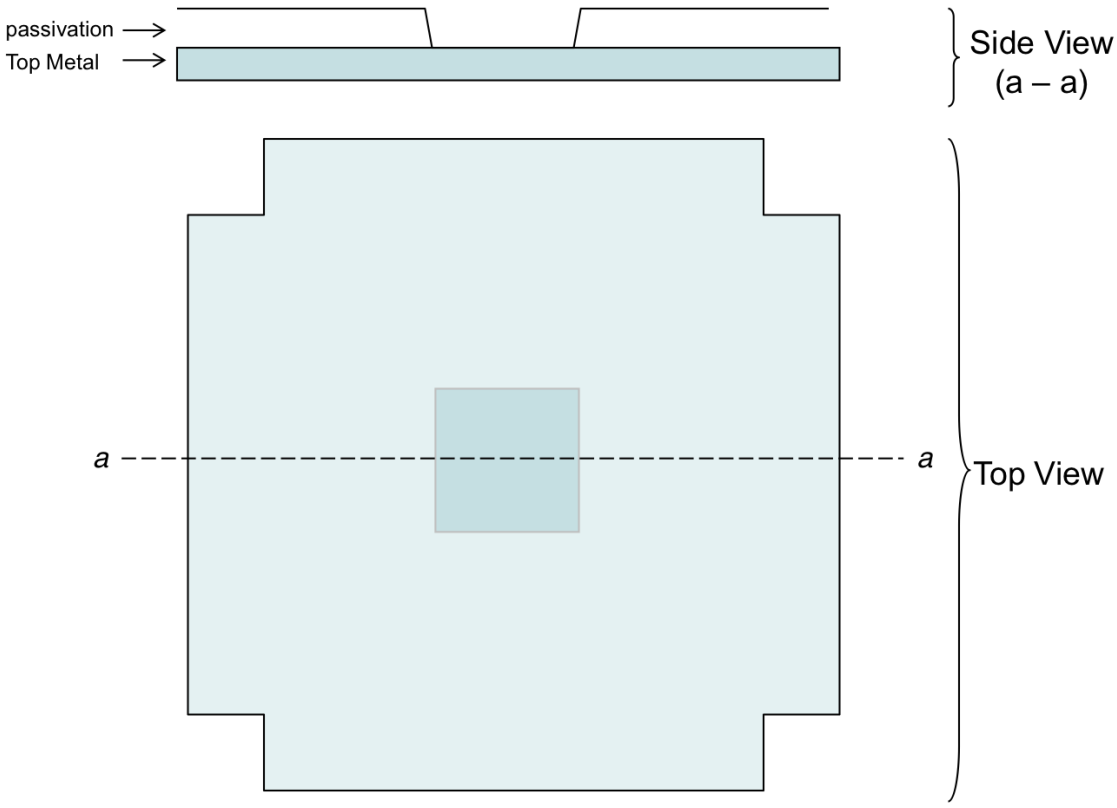
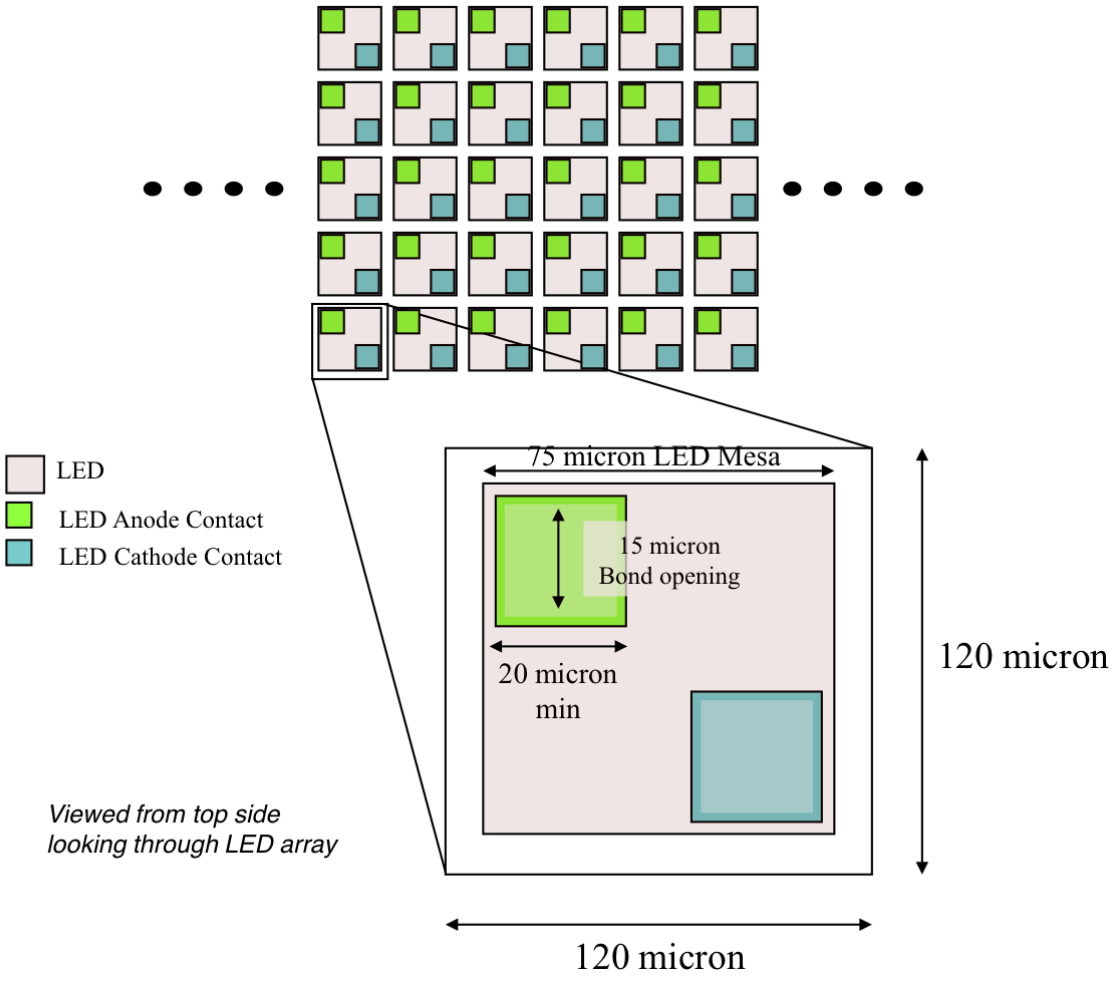


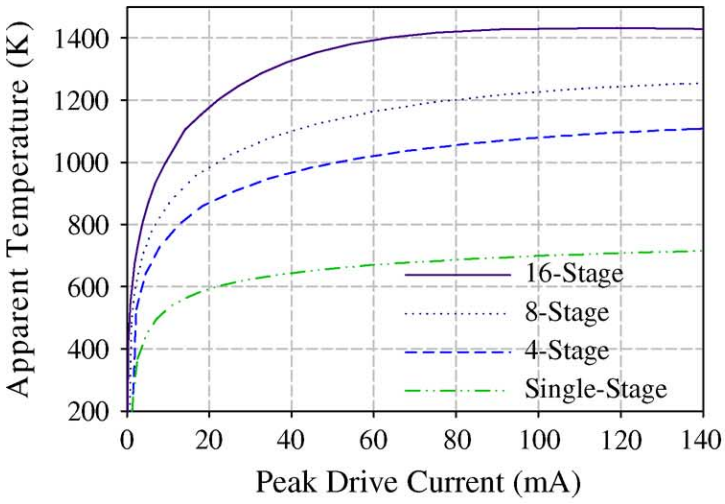
Figure 2.7: SLED array structure



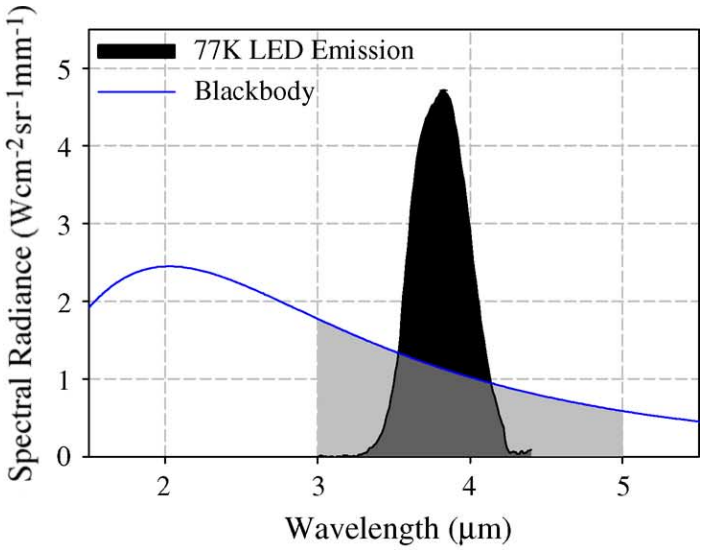
black when cold. Importantly for this project, a black body emits a temperature-dependent spectrum of light and intensity. The thermal radiation emitting from a black body is referred to as black body radiation. If we consider just a band of interest, a black body heated to a certain temperature will emit a corresponding amount of light power. If the infrared emitters, SLEDs in this case, can produce light in that band with the same amount of light power, then emitters are considered capable of creating that same apparent temperature. Again, the emitter is not physically at that temperature – it is simply emitting an infrared signature that would be expected from a black body at that temperature.

The width of band of integration is important for a narrow-band source such as SLEDs. The classic black body source is a wide and flat across the band of interest, so when SLEDs are compared against wide-band sources they are at a considerable power disadvantage; on the other hand, if one narrows the band of integration, the characteristics of the SLEDs technology yields very high apparent temperatures (exceeding 3000 Kelvin) [5]. So the important question is: should emitters only tested against black body sources or should apparent temperature depend on the width of integration of corresponding infrared sensor technology? Testing all infrared technology against black body sources removes confusion and levels the playing field when evaluating diverse infrared technologies. But this does not make sense if the majority of the technologies replacing wide band sources like resistor array are narrow band. In addition, there is a diverse collection of detector technologies that pair with emitters like SLEDs that are narrow-band [4].

To evaluate the SLEDs against maximum apparent temperature, droop, characteristic curve, stability/repeatability, crosstalk, and operability, a 256x256 MWIR camera with a high refresh rate is used to capture the output of the emitters. The way the camera measures intensity is with a bin for each pixel called counts. Counts are not linearly related to apparent temperature and must be calibrated. Taking



(a) Thermal output data of cascaded LEDs



(b) Blackbody equivalent calculation

Figure 2.8: Apparent temperature [3]

into account filters or other losses for a black body source is part of the calibration process.

2.4 Thermal Management

Thermal management for the SLED is highly important because the power output and apparent temperature increases many fold when the devices are cooled from 300 Kelvin to 70 Kelvin [5]. In order to cool the devices down, liquid nitrogen is poured into the dewar reservoir. Inside the dewar there is a cold finger between the reservoir and the socket for the LCC-68 package. When the SLEDs are operating, the heat from devices must travel through the substrate to the bump bonds, through the pads of the driver chip, traverse all seven layers of metal, through the substrate of the driver, into the silver epoxy, and through the ceramic package that touches the cold finger. There is a large amount of thermal resistance resulting in temperature rise across the whole hybridized device. This pushes the SLEDs into a less efficient mode of operation and causes a loss in power. Another important issue is the rise in the background temperature of the SLEDs. When calculating apparent temperature, the power radiated when the chip is off is subtracted from the power radiated when the chip is on and emitting a pattern. Ideally, the device's background temperature would be at or near 77 Kelvin even during operation with ideal cooling.

2.5 Pulsed Mode Operation

Pulse mode operation is a solution to a few operational problems. The LCC-68 is a completely ceramic package with a poor thermal conductance but it does serve as a large thermal mass. By operating the chip with a low duty cycle, the heat emitted does not build up and is removed during the inactive period. This pulsed-mode operation does not allow for all tests to be completed. For example, when testing droop the chip must continue to operate over a longer period of time.

Also, pulsed mode operation does not allow the use of cheaper and slower thermal cameras to examine the output from the SLEDs.

Chapter 3

COMPLETE 68X68 PROJECTION SYSTEM

3.1 SLEDs Test Plan

The first objective after the project restructuring was to design an entirely new testing platform to implement the *SLEDs TEST PLAN* which was a series of tests to be performed by the staff at the Kinetic Hardware In-The-Loop Simulator (KHILS) at Eglin Air Force Base. The purpose of the tests was to gauge the performance of the prototype devices. The characterization included rise time, fall time, maximum apparent temperature, droop, characteristic curve, stability/repeatability, crosstalk, and operability. The first new piece of major equipment associated with the next generation of the project was the Lakeshore Model MTD-121 Modular Test Dewar Cryotest System. The particular dewar was configured for a 68-pin ceramic lead-less chip carrier.

3.2 Bonding Diagrams

It should be noted that the dewar and the LCC package each have 68 pins. The 68x68 RIIC driver has 296 pins which means that certain pins on the chip must either be disconnected or shared with other adjacent pins. The connections are made with solid gold bond wire that connects the pads of a chip to the pads of the lead-less chip carrier. These bond wires are about a 1 mil (1/1000 inch) wide and can vary in length between 100-500 mils. The mapping of the locations and connections of a bond wire is known as a bonding diagram. Making a bonding

Figure 3.1: Lakeshore Model MTD-121 Modular Test Dewar with funnel and mini blue pour dewar

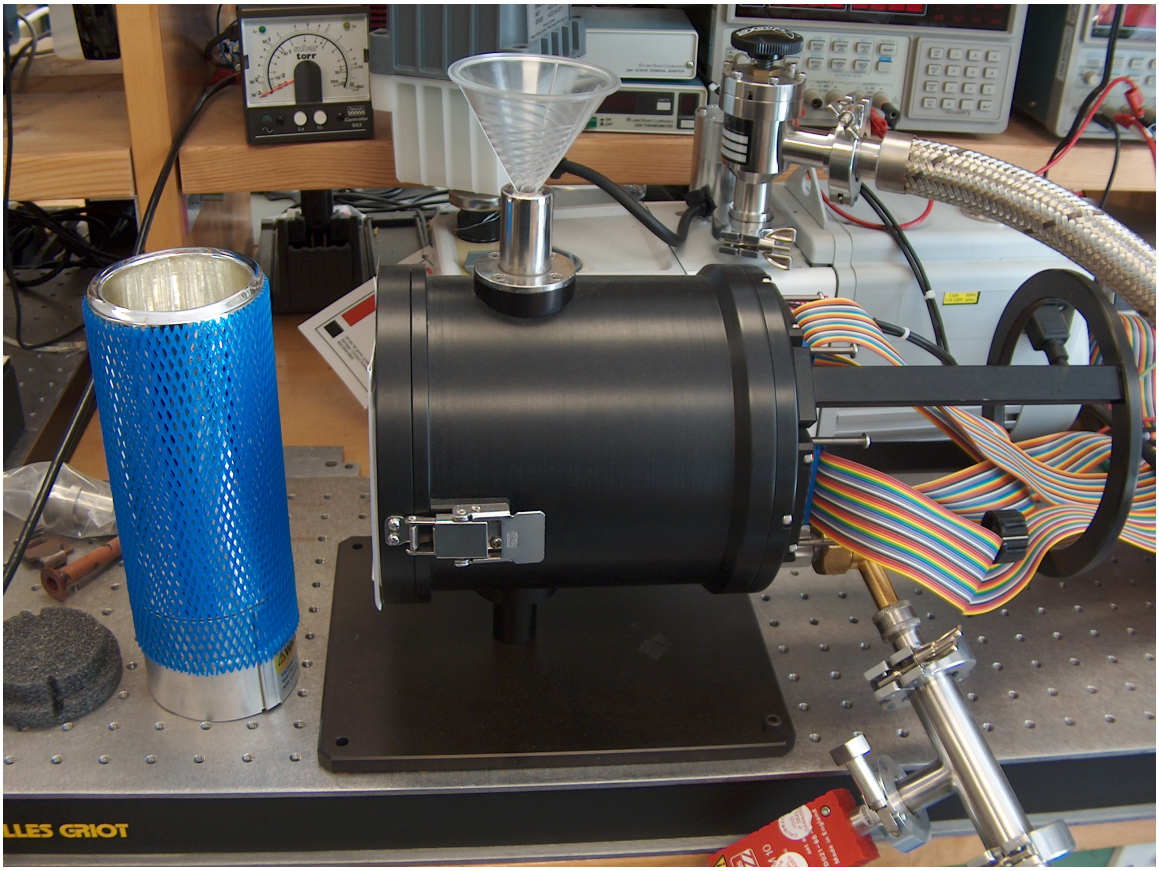


diagram with the pin constraints is a classic optimization problem, and the best bonding diagram depends on which features are optimized.

In order to make a bonding diagram to test yield and operability, the row and column controls for the majority of the chip must be connected in order to activate a corresponding majority of the LEDs. Since the percentage of testable LEDs is the percentage of functional LEDs multiplied by the percentage of mapped LEDs, in order to get a accurate view of operability the percentage of mapped LEDs should be maximized. Another reason to create a *full* bonding diagram is if the particular hybridized device has a low yield. Consider a hybridized device with a 5% yield and only 20% of LEDs mapped; there is a reasonable chance that few or no LEDs would be observed as operational. Since it is often the case that experimental hybridized display devices often have a extremely low yield, this scenario should be considered.

3.3 Test Pins

One footnote feature of the 68x68 SLEDs driver is the inclusion of the test pins. Remember the SLEDs chip is designed to drive LED devices attached to the top of the chip, not through the easily accessible perimeter pads. If one was to drive a single pixel, a probe station tip would have to be placed at the correct bond pad of 4096 to sense the drive voltage. The test pins are a pair of perimeter connections attached to each corner pixel driver and corresponding anode of a SLED. In order for normal functionality, one must short the pair of pins for the corner pixel.

When the pairs of test pins are left open (disconnected), each pad has an important function. The test pad connected to the driver allows you to monitor and verify the voltage generated by the driver to power each pixel. By placing a controlled resistance (or load) between the driver test pad and some lower potential cathode voltage the driver can be characterized with an I-V (current versus voltage) sweep. The other test pad of the pair is connected to the anode of a corner SLED. The cathode side of the SLED is common to all SLEDs. This allows for a direct drive

Figure 3.2: *18x18* bonding diagram

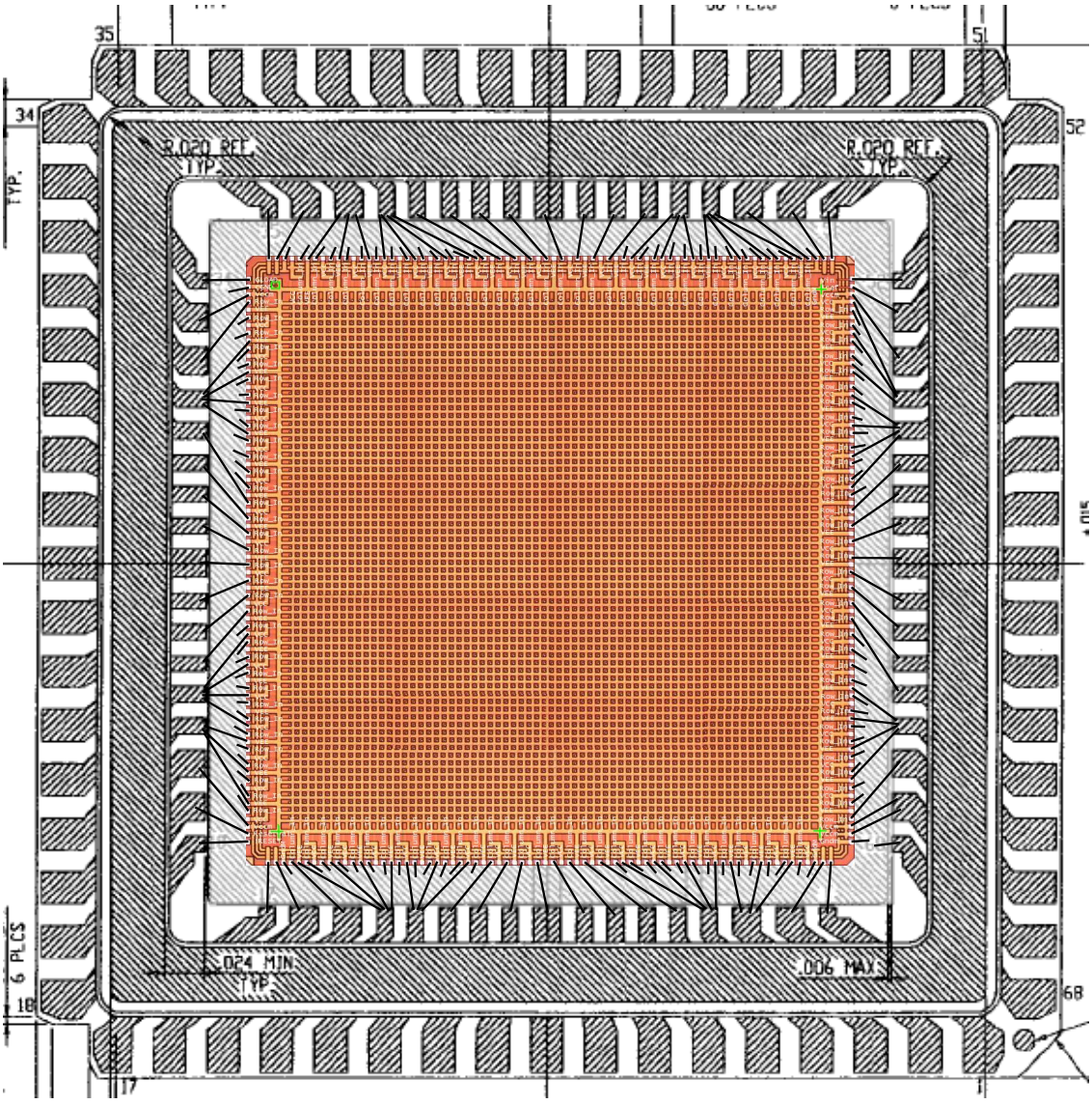
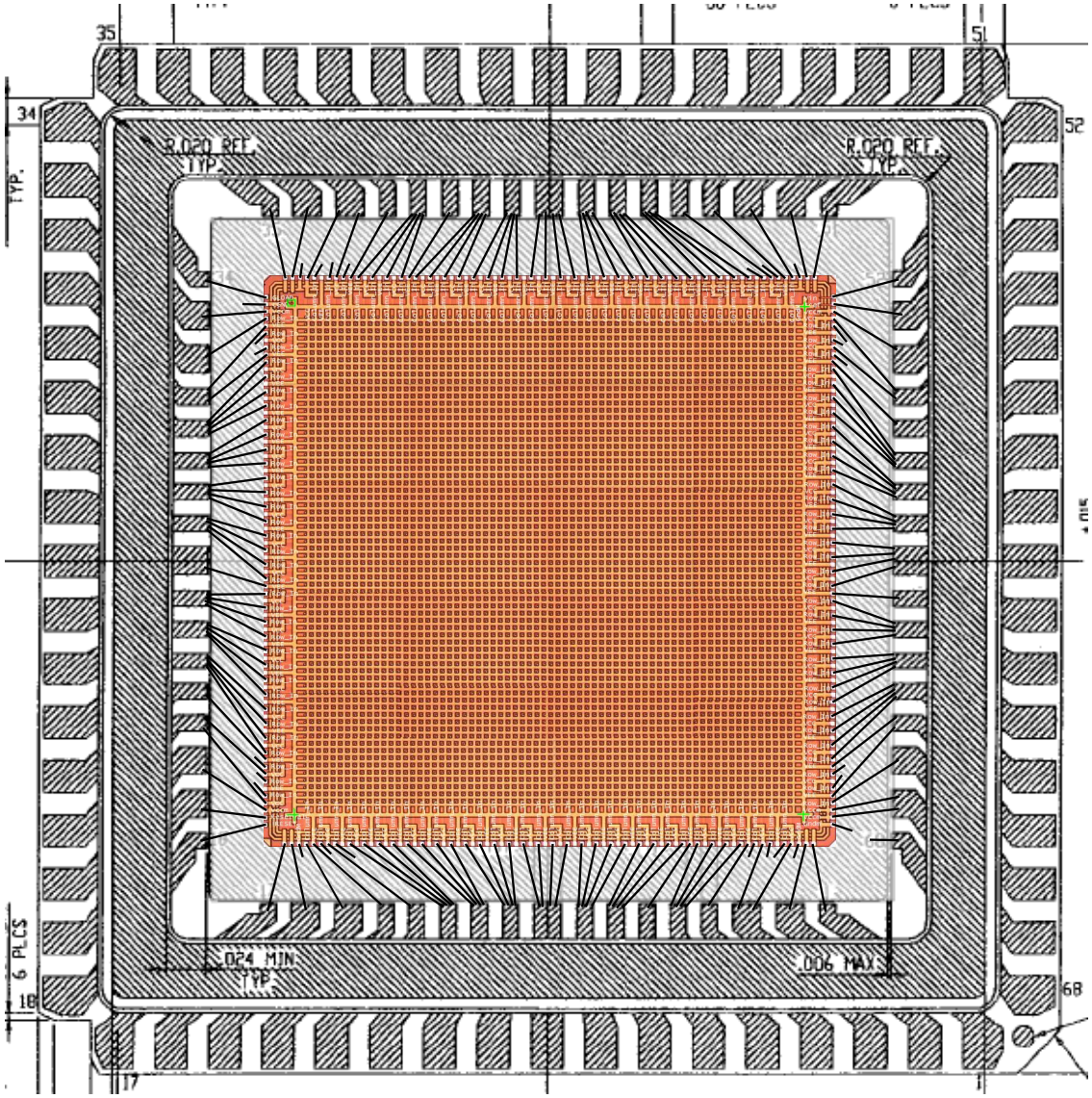


Figure 3.3: *Full* bonding diagram



through the corner pixel with a source meter. This allows separate characterization of the driver chip and the SLEDs chip in a hybridized configuration for each corner.

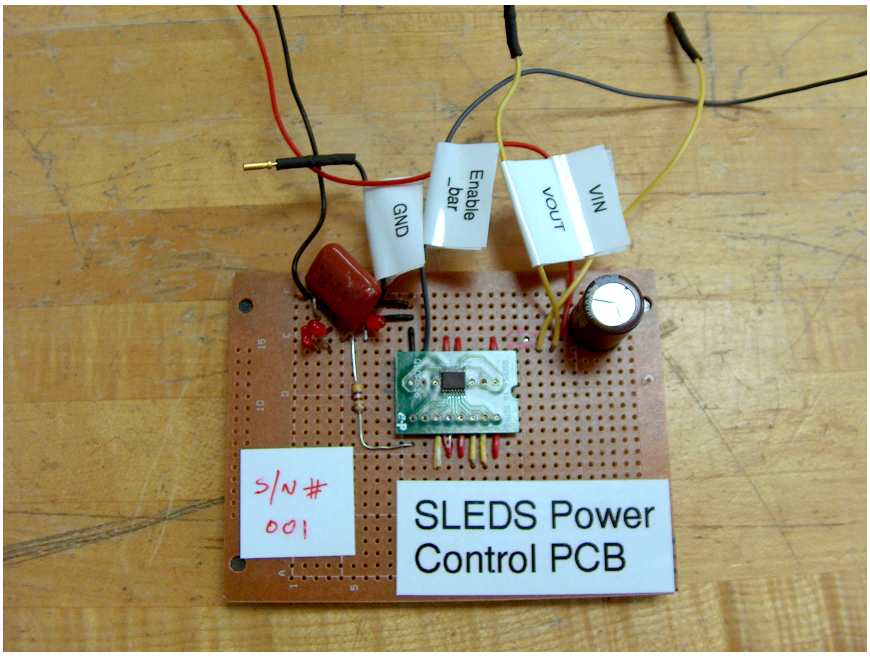
From the perspective of a chip designer, the corners of the driver are the easiest and most logical location to add test pins. During the hybridization process, which includes bump-bonding and deposition, corners are often made less reliable or inoperable. This is general knowledge among the professionals in opto-electronic packaging but not those typically involved or contracted to design custom application-specific integrated circuits (ASICs).

3.4 Power Control Circuitry

Prior to the first KHILs testing trip with the second CVORG designed test system, a large standby power consumption was noticed during testing. This large power consumption was caused by a 20K ohm resistance on each pixel; in parallel, this resistance is equivalent to less than 5 ohms. When the negative VEE (the voltage on the common cathode of the arrays) was lowered to increase the voltage difference across the device, it also allowed several amps of current to flow even when all pixels were driven off.

To mitigate the problems caused by this large standby current, Nick Waite conceived of using external power control circuitry. This device would integrate with the existing FPGA board to only enable chip power during a pixel display sequence. This solution decreased the temperature rise associated with the power burned through the simmer resistors. However, it did not help the voltage drop on the supply voltages and the current limiting from our power supplies. To compensate for these, large capacitors were added to the voltage supplies to provide the necessary current to drive the display sequence. Ultimately this solution allowed us to complete a relatively successful test of the hybridized SLEDs design, however, not reaching the maximum potential results because of the power robbed by the simmer resistors. The resistors had to be removed, unfortunately requiring the driver chips to be

Figure 3.4: Power control board



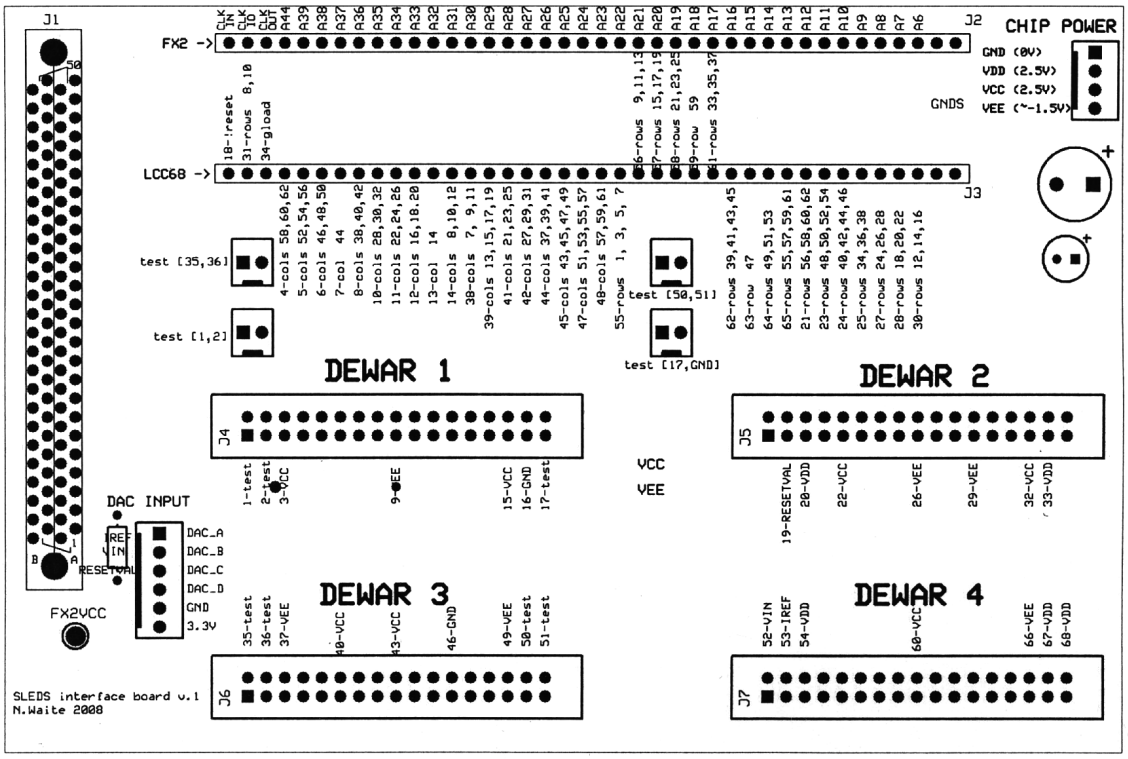
remanufactured. After receiving the chips back, the decrease in standby power consumption was verified.

3.5 Interface PCB

After deciding to use an FPGA to control the digital and analog inputs of the driver, an interface between the driver chip and our control system was designed. This board would combine the connections from the dewar, the digital and analog outputs from the FPGA, and the power supplies. The dewar connects to the PCB using four IDC 34-pin connectors, similar to those used in floppy drives. Half of these pins are grounded, which gives a total of 68 pins. The digital outputs from the FPGA were connected to the PCB using a Hirose 50-pin FX-2 connector. The FPGA's analog outputs were connected to the PCB using a 6-pin, single-row 100 mil spaced header. Power was provided to the board using mini-banana connectors. This board

required some modification after fabrication due to power and ground shorting. The PCB interface board functioned properly for the duration of the testing, but several improvements were applied to the next iteration of board. Integrated power control circuitry, reconfigurability for bonding diagrams, and additional headers for probing were added to the second generation PCB.

Figure 3.5: PCB outline showing traces connectors and labels



In designing the software control system, a decision had to be made to choose an architecture for the control system. One option is using a micro-controller. They have shorter software development times because they are coded in C or other high-level languages. The disadvantage of micro-controllers is their single-threaded nature, which only allows one operation to be executed at a time. The other option

Figure 3.6: Photograph of actual board. Note the lack of soldermask or silkscreen typical of prototype boards.

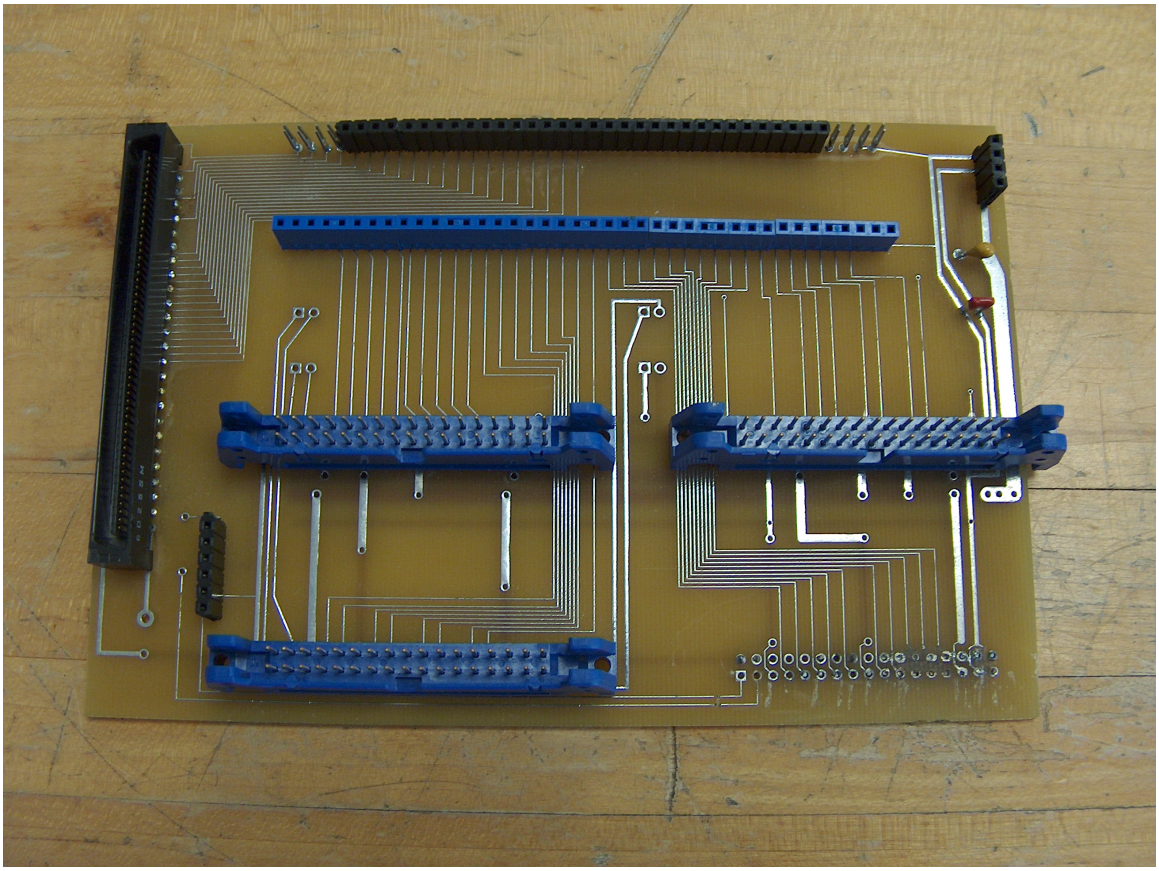
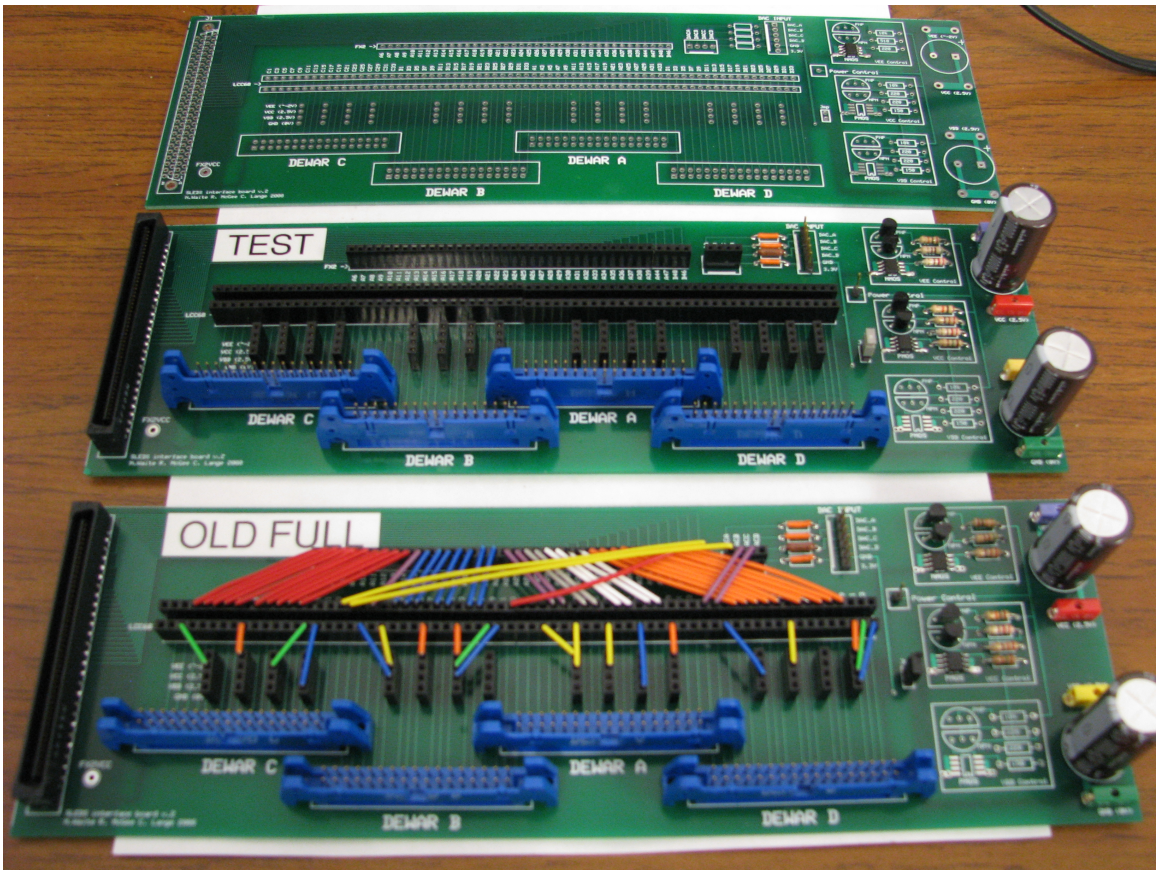


Figure 3.7: Second generation interface board with integrated power control circuitry



is using a full VHDL FPGA implementation of the software control system. VHDL is essentially a parallel software language that allows fully independent and well-timed execution. Due to the complex nature of these relationships, the software development time is often longer than equivalent C programs. The advantage is increased performance and precisely timed concurrent events and operations.

Weighing these factors, it was decided to use a mixed architecture called Unified Logic from Eridon, a software development kit (SDK) designed for embedded systems. It provides a built-in application programming interface (API) for many of the devices found on the FPGA demonstration board. The software allows modules to be snapped together quickly and allows for the utilization of the built in devices programed in high-level languages. From the C code, one can make calls into HDL device drivers, which are executed in parallel. Unfortunately, Eridon no longer offers this software for sale, but since the Xilinx Embedded Development Kit (EDK) has matured significantly the uniqueness and necessity of the Eridon software package has decreased.

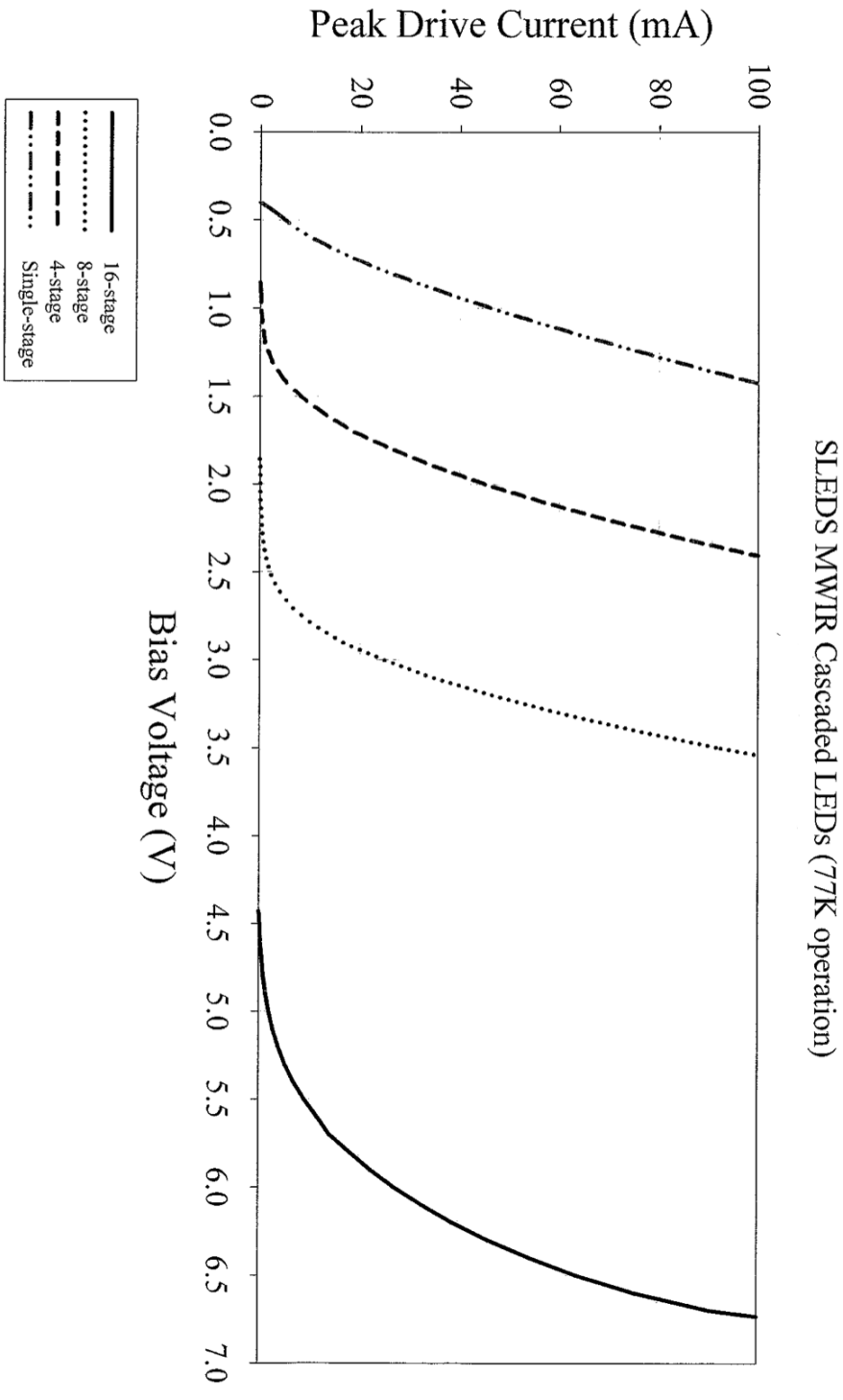
The FPGA board that was selected to be used to control emitters was the Digilent's Xilinx Spartan 3E FPGA demo board. It was chosen because of the large number of GPIO (general purpose Input/Output) pins, familiarity with this particular board, preexisting hardware, and existing test infrastructure. Initially, SLEDs testing started using a digital analyzer for the digital input signals and a separate analog scope for analog inputs and outputs. This proved to be problematic as it is difficult correlate time-domain signals without a global clock. In this situation, a high-speed mixed signal oscilloscope with a wide digital input bus was the ideal piece of test equipment.

3.6 Swing

What happens when the device specifications do not match the device's true requirements or its future requirements? Communicating objectives and design

targets with terse unscientific specifications or even a complex specification book is often problematic in projects of this complexity. The problem is when a third party gives specifications to the first party, but the second party is the end user of the product is left without input into the design process. One of the primary problems with the design of the 68x68 driver was the insufficient swing voltage. Swing, in this case, is the amount of voltage change across the LED at minimum drive voltage and maximum drive voltage. In other words, the driver was able to bias the chips at voltage but without significant voltage headroom. By changing the *Vin* signal from 0 - 2.7 volts one would see a change in drive voltage swing from 0 to 1.5 volts. Through a combination of power supply voltage increases and careful biasing, more swing was squeezed from the existing design – finally pushing the swing to a maximum of 2 volts. To determine proper biasing, see Figure 3.8. The voltage should start from before the bend in the diode curve and ending at the voltage level giving the desired current. For a 16-stage SLED the low voltage should be set around around 4.5 volts and go up to 6.75 volts implying a desired swing of 2.25 volts.

Figure 3.8: Cryogenic SLEDs voltage/current curve [3]



Chapter 4

TESTING THE COMPLETE SYSTEM

4.1 First Test of 68x68 System

During the first trip to demonstrate and benchmark the technology at KHILS, many valuable lessons were learned. It was the first time the chip was operated using the drive electronics and simultaneously observing light output. All of the preparation and design for the system surrounding the emitters was done without any measured light output. As we learned latter in the program, a characteristic SLED voltage-current curve is not an indication of light output. In addition to operating blind, the complete system had never been tested at cryogenic temperatures. When a complex electronic system is cooled several hundred Kelvin, many modest changes can add or multiply to create an entirely different normality.

Once the liquid nitrogen fills the dewar, the chip cannot be removed until all the liquid nitrogen is backfilled and the temperature rises inside the dewar. Otherwise, the difference in temperature will cause condensation to form inside the dewar. Consequently, quick swapping between parts cannot be performed and testing may be limited to testing one chip a day depending on the particular setup.

4.2 Second Test of 68x68 System

Before the first test at KHILS, all testing was completed without light detection or cryogenic temperature. After the mixed results of the first testing session,

new pretest procedures to verify light output and cryogenic functions were implemented. Before testing the device at KHILS for the second time, the device was tested in-house to determine the configurations to maximize light output.

Tests evaluating rise time/fall time, maximum apparent temperature, characteristic curve, stability/repeatability, and crosstalk often require control over a single pixel or precise number of pixels. The SLEDs 68x68 driver is completely asynchronous so the signals must be carefully ordered to active pixels on the chip. In addition to the digital signals, the chip has several critical analog inputs that must settle before their value is sampled. The analog inputs should not go above the digital power voltage because in certain situations it can cause *all* the SLEDs to activate. 100% activation is problematic because the chip can only properly power ten or twenty percent of the array at full power.

The following figures are screen captures from a Tekronics MSO 4034 mixed signal oscilloscope and a single element MWIR detector. The first Figure 4.1 shows a good strong light output after tweaking all the voltages. The second Figure 4.2 is problematic because light output occurs prematurely when *Vin* is enabled instead of occurring when the load signal is enabled. This means that the voltage *Vin* was high enough to overrun the transistor and activate all LEDs causing significant uncontrolled light output that consumed all the power and drained all the capacitors. This is observable by the sag in the green line over time. The third Figure 4.3 shows the correct sequence of commands were light corresponds to the load signal.

Figure 4.1: Maximum controlled output

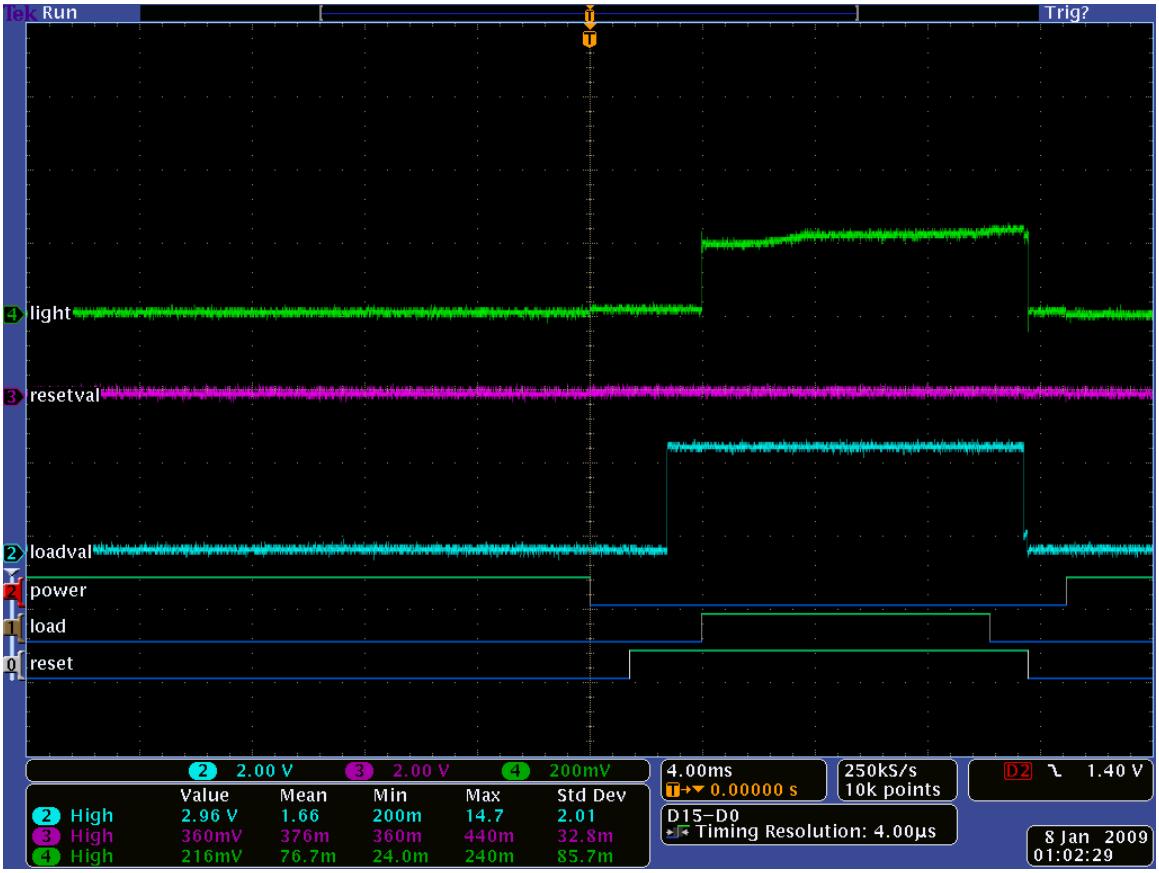


Figure 4.2: Uncontrolled output caused by over-voltage on *Vin*

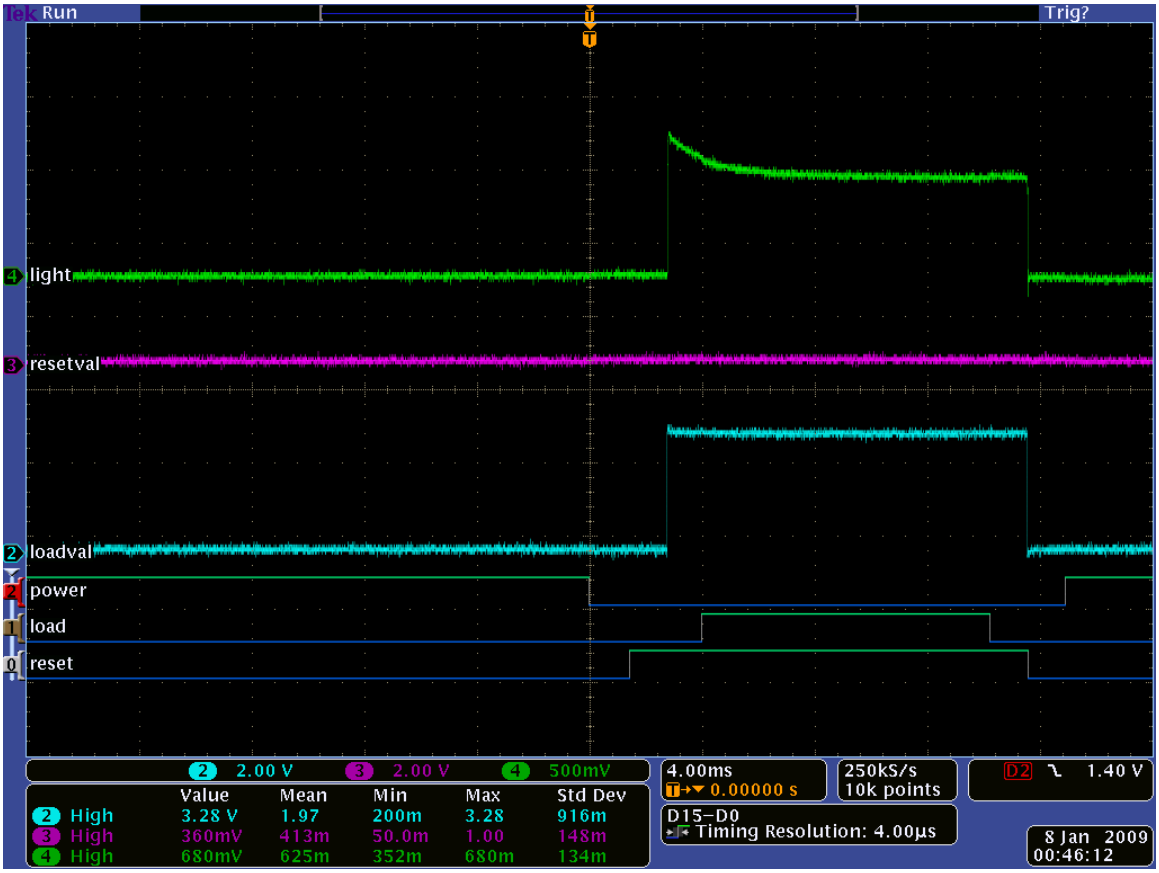
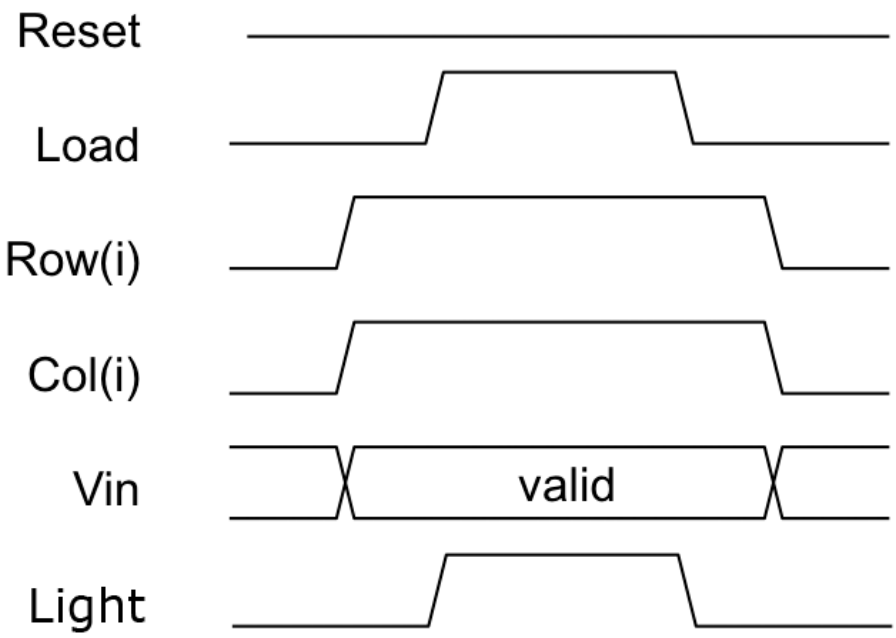


Figure 4.3: Correct sequence to fire pixels and corresponding light output



Chapter 5

RESULTS

5.1 Array Testing with MWIR Camera

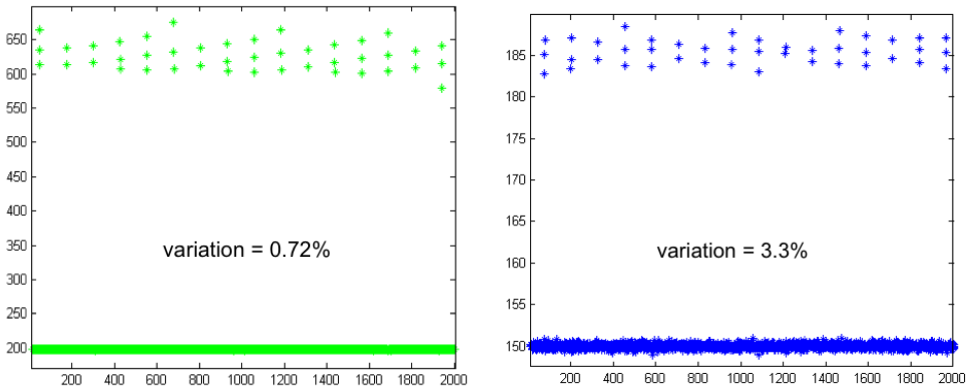
The following are the results from the array testing at KHILS at Eglin Air Force Base in Florida that took place during February 2-5, 2009. KHILS provided definitive measurements of the performance. The *full* and *18x18* MWIR array were tested at room temperature and cryogenic temperatures. These results well-exceeded previous testing and marked a major milestone in the development of SLEDs as an IR projection system.

5.1.1 Stability/Repeatability

To record the stability and repeatability of the SLEDs, the camera records the radiometric output of the emitters over time and each array was pulsed at 100% drive voltage at cryogenic temperature. An array that is considered stable is expected to measure the same number of camera counts each time. The stability was calculated by subtracting the background temperature then taking the standard deviation of the peaks and dividing it by the mean. See Figure 5.1.

5.1.2 Crosstalk

Thermal crosstalk between emitters can be measured using a macro lens with an IR camera to more clearly resolve individual emitters. The camera counts of the two on emitters were measured, as well as the spacing between the brightest camera pixels. This spacing was used to measure camera counts at off emitter locations.



(a) *18x18* subarray results (b) *Full* subarray results

Figure 5.1: Stability results for two types of MWIR arrays

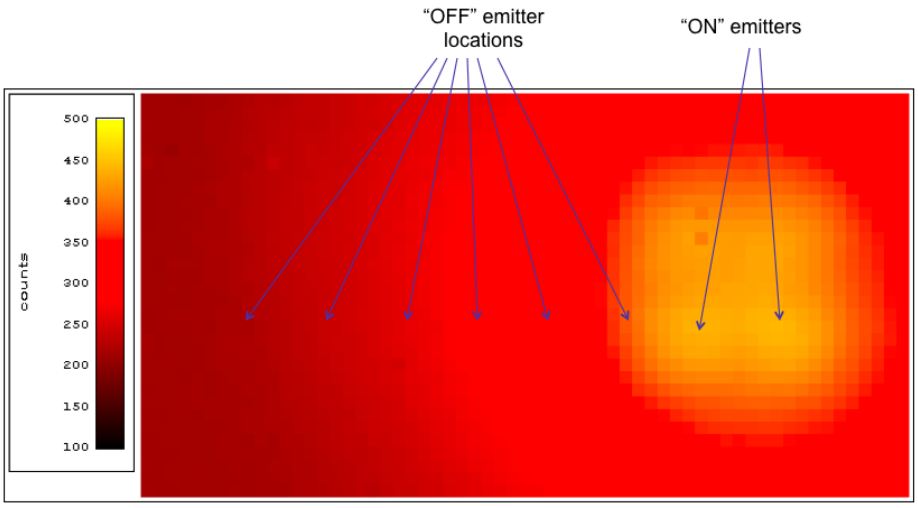
Since as the radiance is measured at equal points away from the two on emitters, the value falls off smoothly (i.e., without any peaks at the locations of the OFF emitters) to background level as seen in Figure 5.2. According to the results, there is no measurable thermal crosstalk.

5.1.3 Characteristic Curve

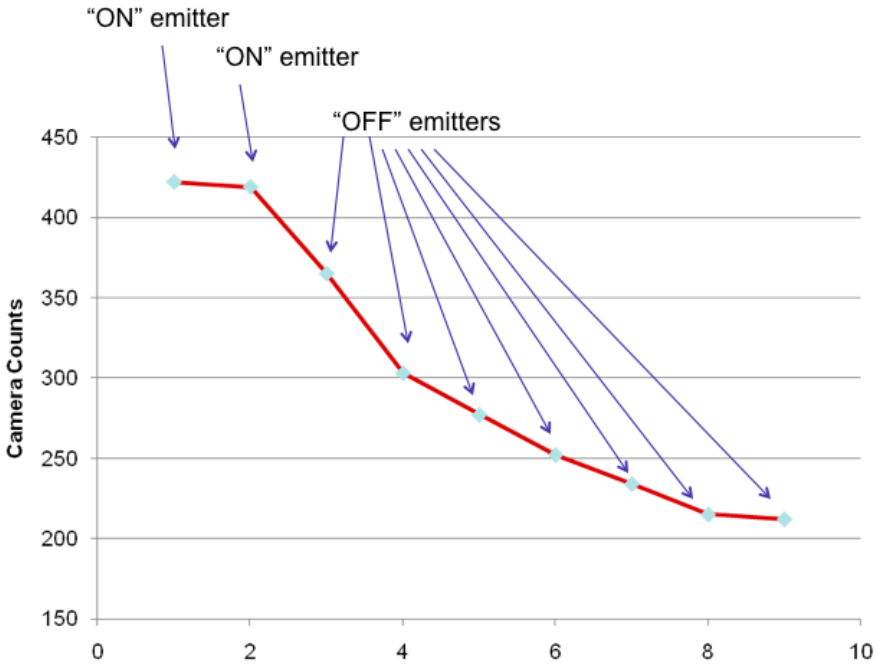
In this test, the devices were driven in steps from 0% to 100% drive voltage at cryogenic temperature. In Figure 5.3 the correlation between input voltage and output light is evident.

5.1.4 Maximum Apparent Temperature

Determining the maximum apparent temperature was one of the most important parts of the testing process. In Figure 5.4, part B, a single pixel maximum apparent temperature was recorded at 1004 Kelvin. In Part A, a block of 4 adjacent emitters yielded a value of 960 Kelvin.

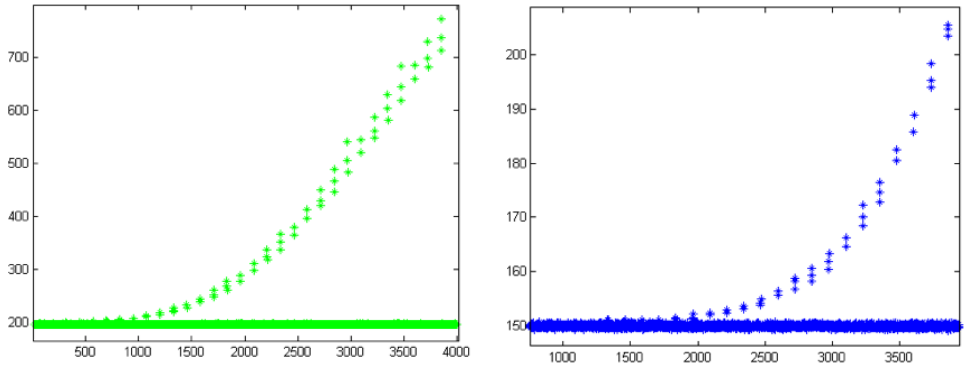


(a) 2D heat map



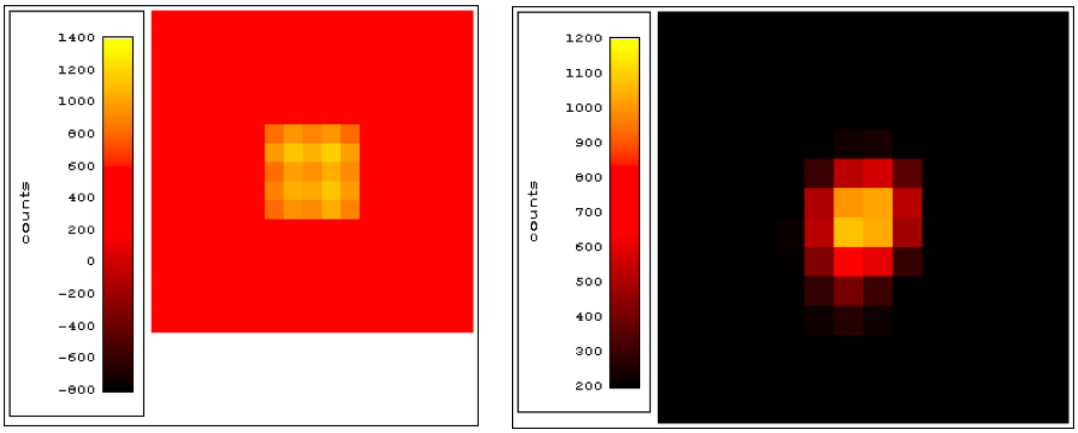
(b) Temperature versus distance from hot array

Figure 5.2: Crosstalk measurements



(a) *18x18* subarray results (b) *Full* subarray results

Figure 5.3: Characteristic curve measurements



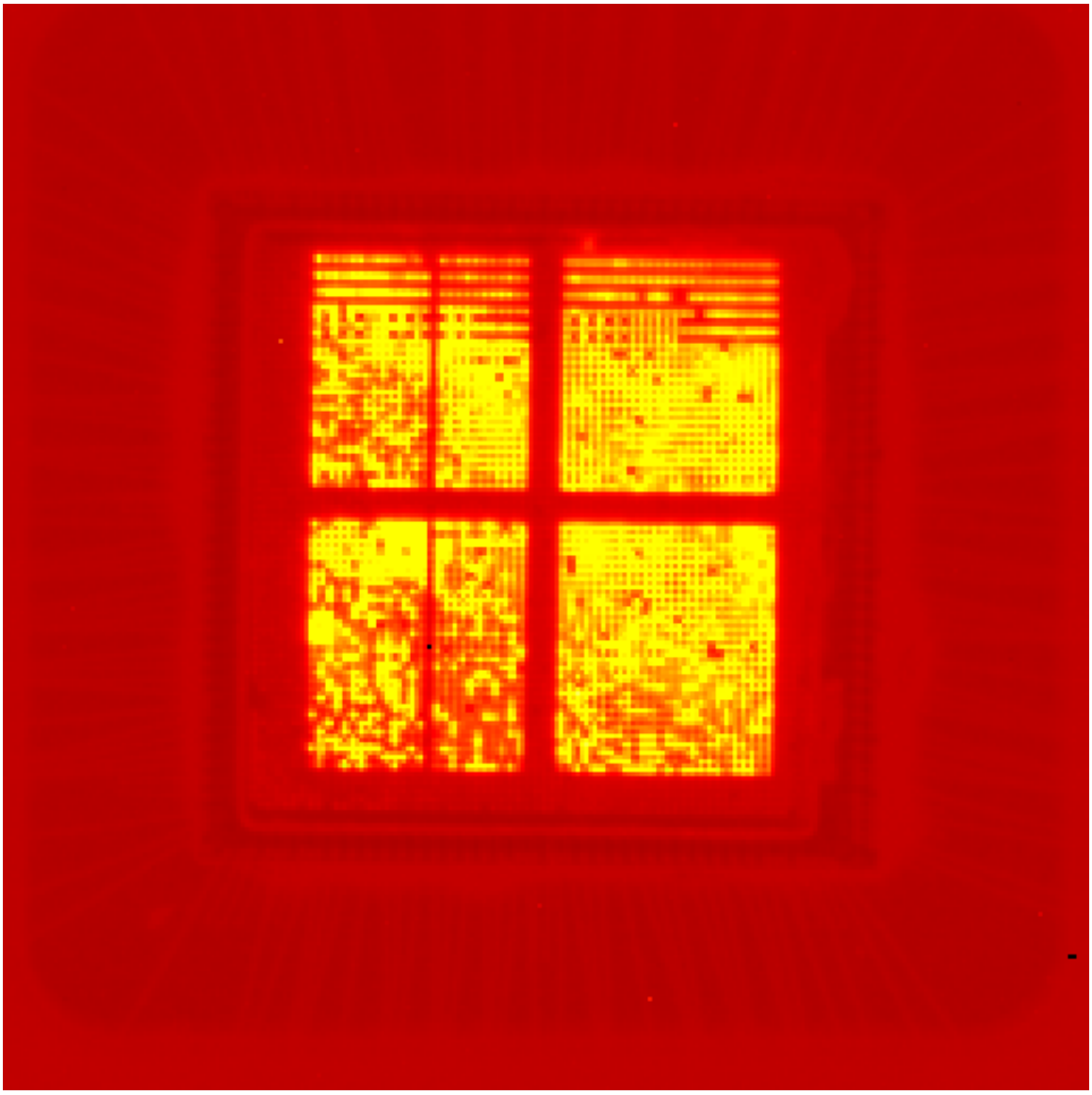
(a) 2z2 subpixel (b) Single subarray

Figure 5.4: Maximum apparent measurements

5.1.5 Yield

In these types of experimental devices, yield is often very low. See Figure 5.5. Note that the cross in the middle is purposely nonfunctional because the row and column controls are unconnected. It was determined that the yield for the *full* array was around 90%.

Figure 5.5: Merged output from *full* array showing yield



Chapter 6

FUTURE WORK

6.1 LWIR

The next benchmark is testing the mature 68x68 projection system with new devices that emit in the LWIR (long-wave infrared) instead of the MWIR (mid-wave infrared). Although the new LWIR arrays are significantly different from the MWIR, little will change with the drive electronics. The new devices will require smaller swing voltages and slightly less current. After testing the LWIR devices, the 68x68 projection system will be retired.

6.2 512x512

Currently under development is a significant advance in resolution, maximum apparent temperature, and system complexity. The new projection system will have a resolution of 512x512. This is 64 times the number of pixels and is an increase of almost two orders of magnitude. Because of added row and column decoders on the new 512x512 chip, the chip has more power pads than digital control pads. A new driver had already been fabricated and is currently being tested. The new system will have all new software, interface boards, drive electronics, and LED design. Some custom chip packages have already been created to replace the LCC68 and dewar modifications to accommodate the new chip. Powering and cooling the chip will require significant engineering to be capable of sustained emission with a useful percentage of SLEDs powered. Most importantly, this system will be the first to be capable of application in the field.

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