BUILDING AN OPTIMIZED PASSIVE OPTICAL COMPONENT LIBRARY FOR SILICON PHOTONICS PLATFORM

by

Yangjin Ma

A dissertation submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical and Computer Engineering

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It is hard to imagine how much I have learned and grew during the past few years working in this world-class group with a group of top experts in silicon photonics.

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ABSTRACT

Silicon photonics has been intensively investigated in the past decade and has now become a promising platform for optical operations in light generation, routing, modulation and detection. One of the most important applications is integration in fiber communication systems with the potential to further reduce costs while improving the performance.

Although active components such as modulators and detectors are crucial, small passive components that seem trivial are actually vital in high complex and high-density system level integration. On the one hand, small performance improvements in each passive component may aggregate quickly and make huge advantage for active components. On the other hand, well-performed passive devices may save a significant amount of extra controlling effort on the chip to improve energy efficiency and reduce cost off the chip.

In this thesis, a comprehensive design work of passive Si photonics components will be presented, starting from basic building blocks such as waveguide crossing, y-junction, to application-specified devices for wavelength routing and polarization handling. Then systems such as a four-channel polarization insensitive wavelength-division multiplexing (PI-WDM) receiver enabled by such passive components will be discussed in detail. Performances beyond state-of-the-art have been achieved in most cases.

Chapter 1

INTRODUCTION

1.1 The State Of Silicon Photonics

Over the past decade, the silicon photonics community has made fantastic progress from academic research and development to a turning point of production and commercialization.

Inherent from the electronics industry, silicon processing such as lithography and dopant recipe has already been very mature, which makes the fabrication of silicon photonics devices very reliable in the first place. The dominant silicon photonics platforms are based on silicon-on-insulator (SOI) material system, where the oxide layer offers a buffer layer that prevents light from leaking away. Meanwhile the high index contrast between silicon and silicon dioxide (SiO_2), 3.48 vs 1.45 at 1.55 μm, enables tight confinement of optical modes, which effectively shrinks the device footprint. Very complex and compact systems can potentially be built on such a platform at a low cost. The bandgap of silicon is 1.12eV, which is transparent in the near IR wavelength range. Silicon has excellent optical properties within the optical communication wavelength regime (1.3-1.6um wavelengths).

Despite of its excellent properties in guiding light, silicon is not a good material for electro-optical operations needed in optical communications where strong electron-photon interactions are desirable. Due to the centrosymmetry, no second order nonlinear effect exists in crystalline silicon. The third order nonlinearity of silicon is also too week for lots of applications. These two drawbacks fundamentally

limit crystalline silicon from applications in electro-optical modulations and all optical operations. [1] Moreover, the light emission in silicon is also fundamentally inefficient due to its indirect bandgap nature.

For a long time, III-V semiconductors such as InP, and electro-optical materials such as Lithium Niobate (LiNbO3) were widely considered to be the most viable material systems for integrated optics. III-V compound semiconductors like InP benefit from a direct band structure and proper bandgap for light emission. Even today, they form the basis for most of the photonics components in use for metro and long-haul communications. The state of the art technology for EO modulators for long-haul data communication applications is based on LiNbO3 due to its large Pockels effect. [2] However, one big limitation for such materials is the expensive substrate, low fabrication yield and, in the case of Lithium Niobate, large footprint.

The first electroopitical effect in silicon, which is known as the free carrier dispersion effect, was reported in 1987 by Soref et al. [3] It was demonstrated in that paper that the change of carrier densities in doped silicon can introduce noticeable refractive index change. Although not a strong effect, it enables design of electro-optical modulator. The first multi-Gb/s capable silicon Mach-Zehnder (MZ) modulator was reported by Liu et al in 2004. [4] The first micrometer scale modulator enabled by silicon ring resonators was reported by Xu et al in 2005. [5] Since then great progress has been made in silicon modulators. Today's state-of-the-art silicon modulators operates at 40 Gb/s, with EO bandwidths of 25 GHz or higher. [6–11] Very high speed MZ modulators (70 Gb/s) [12] and ultralow power ring modulators (0.9 fJ per bit) have been reported very recently.

High quality epitaxial grown germanium (Ge) on top of Si (Ge-on-Si) enables high-speed photodectors on SOI platform with CMOS compatible fabrication process. [13–18] 40 Gb/s or higher operation have been reported. Silicon lasers [19] with either top-down hybrid evanescent coupler architecture [20] or edge-coupled external cavities [21,22] have been successfully demonstrated, filling the last missing piece of an entire platform for system level integrations.

Cisco has launched a 100 Gb/s LR4 transceiver, consists of silicon modulators, WDM (wavelength division multiplexing) multiplexer and co-packaged laser sources as well as driving ASIC. Luxtera also announced 100Gb/s solution based on four lane parallel architecture. For metro and long haul communication, Acacia has announced a 100 Gb/s coherent transceiver, whose optical engine is fully contained in a monolithic silicon photonics circuit. [23] Bell Labs has also demonstrated transmitting112 Gb/s PDM-QPSK (polarization-division-multiplexed quadrature phase-shift keying) signal over 2560-km standard single-mode fiber based on silicon photonic coherent transmitter and receiver. [24]

In parallel with the production effort driven by the industrial players in optical communication, great amount of academic research works are on going. Similar to the electronics industry, fabless silicon photonics foundry services [25–27] emerged and quickly became important for academic groups (and also for companies who want to take in part of this technology) to get access to the world-class CMOS silicon photonics fabrication facilities to realize their creative ideas.

Beyond optical communications, there are a huge number of new applications being explored in both the commercial and academic worlds for this technology. These include nano-optomechanics and condensed matter physics [28], nonlinear

optics [1,29], light detection and ranging (LIDAR) systems [30], very long wavelength integrated photonics [31], quantum optics, novel material integrations such as grapheme [32], and many more.

Stimulated by the promising future of diversified photonic applications on the SOI platform, high-performance low-loss passive components such as routing waveguides (0.026 dB/cm) [33], Y-junctions (0.1 dB) [34,35], waveguide crossings (0.02 dB) [36], grating couplers (1dB) [37,38], etc. have also been successfully demonstrated within CMOS compatible optical lithography process.

1.2 Outline Of This Thesis

The contents of this thesis come from the works that I have done with the OpSIS (Optoelectronic systems integration in silicon) project. Since the very beginning I joined the nanophotonics group, I have been working on the OpSIS project, which provides shared MPW (multi-project wafer) services that are open to all the photonics designers from academic to industry around the world.

Part of my works has been integrating my research interest to the need of PDK (process design kit) development of the OpSIS-IME silicon photonics platform. My research focused on the passive components, which are the major contributions of this work.

In this thesis, I will first go through the basics of silicon photonics platform, classification of passive components and the test setups we used for testing in Chapter 2, to give a general sense of the theoretical and experimental basics needed in this work. I will then discuss in detailed the passive components that I developed during the OpSIS project, including two most fundamental building blocks (Chapter 3) – waveguide crossing and Y-junction – and some novel application-specified devices

(Chapter 4) from wavelength division multiplexing to polarization splitting and rotating.

Besides maintaining and adding PDK components to the OpSIS-IME platform, I have also taken advantage of the active components of this platform and demonstrated high-speed data transmission for both modulators and receivers designs, which are discussed in Chapter 5.

1.3 Publications Related To This Thesis

This section lists the publications directly related to this work. A full list of publications is included in Appendix A**.** Agreement of reprint permission policy is provided in Appendix B.

1. **Y. Ma**, Y. Zhang, S. Yang, A. Novack, R. Ding, A. E.-J. Lim, G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "Ultralow loss single layer submicron silicon waveguide crossing for SOI optical interconnect," Opt. Express 21, 29374–29382 (2013).
2. **Y. Ma**, P. Magill, T. Baehr-Jones, and M. Hochberg, "Design and optimization of a novel silicon-on-insulator wavelength diplexer.," Opt. Express 22, 21521–8 (2014).
3. H. Guan*, **Y. Ma***, R. Shi, A. Novack, J. Tao, Q. Fang, A. E.-J. Lim, G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "Ultracompact silicon-on-insulator polarization rotator for polarization-diversified circuits.," Opt. Lett. 39, 4703–6 (2014). [* Equal contributions]
4. **Y. Ma**, Z. Xuan, Y. Liu, R. Ding, Y. Li, A. E. Lim, G. Lo, T. Baehr-jones, and M. Hochberg, "Silicon Microring Based Modulator and Filter for High Speed Transmitters at 1310 nm," IEEE Opt. Interconnect Conf. MC6, 23–24 (2014).
5. Z. Xuan, **Y. Ma**, Y. Liu, R. Ding, Y. Li, N. Ophir, A. E.-J. Lim, G.-Q. Lo, P. Magill, K. Bergman, T. Baehr-Jones, and M. Hochberg, "Silicon microring modulator for 40 Gb/s NRZ-OOK metro networks in O-band.," Opt. Express 22, 28284–28291 (2014).

6. **Y. Ma**, L. Yang, H. Guan, A. Gazman, R. Ding, Y. Li, K. Bergman, T. Baehr-Jones, and M. Hochberg, "Symmetrical polarization splitter / rotator design and application in a polarization insensitive WDM receiver," Under Review

Chapter 2

THEORETICAL AND EXPERIMENTAL BASICS

2.1 Silicon Photonics Platform

Silicon has been extensively studied in the past decade for to manipulate photons on chip. As stated in chapter 1.1 , individual devices from light generation, modulation, detection to detection have already been demonstrated, showing great capability of developing a monolithic platform to construct high-complex systems.

Major silicon photonics platforms gravitate toward to two types of SOI thickness: multi-micron SOI (usually 3um) with low-confinement modes [39,40] and submicron SOI (usually 220nm, 250nm, or 300nm) [37,41–43]. For multi-micron SOI waveguides, polarization independent circuits can be built due to low confinement of optical modes. However, it requires very large bend radius (250 μm in [44]) to avoid excitation of higher order modes. This type of silicon photonics platforms become less promising when it comes to dense and energy efficient photonic integration using devices like micro-ring modulators [45,46].

Presently, submicron platforms are emerging as the dominant ones for large-scale integration. The width of a single mode waveguide in such platform is usually ~2 times larger than its thickness in order to provide strong mode confinement, thus enabling tight bends (radius <2.5 μm in [45]).

All the works in this thesis, if not mentioned specifically, are based on the OpSIS-IME silicon photonics platform that I participated in building and maintaining. The silicon-on-insulator (SOI) thickness is 220nm, with 2 μm buried oxide (BOX),

three etch steps and two back-end-of-line metal layers, fabricated with 248 nm optical lithography. [47]

Figure 2-1 (a) shows an SOI silicon photonics platform, where on/off-chip couplers such as grating couplers, passive components such as waveguides, modulators and Ge-based detectors are monolithically integrated. Figure 2-1 (b) is a picture of an 8-inch SOI wafer with various components and circuits fabricated out of the same process design kit (PDK) library provided by the SOI platform.

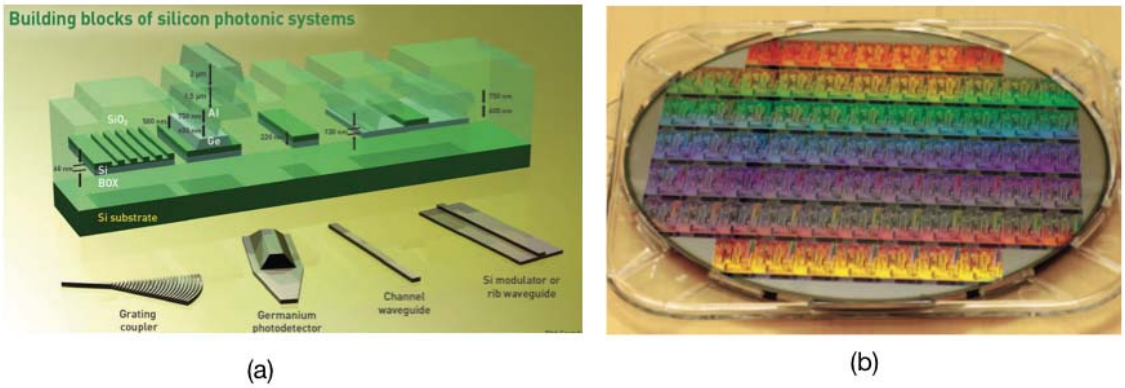

Figure 2-1. (a). (From [48]) 3D rendering of an SOI photonics platform, showing key building components: grating couplers, waveguides and Ge-on-Si photodetectors. (b). (From [49]) An 8-inch SOI wafer with various photonic components and circuits.

2.2 Classification Of Passive Components

Generally light has four dimensions inside a photonic integrated circuit (PIC): intensity (power), phase, wavelength and mode (polarization). Design and engineering of on-chip passive components typically fall into either one or more of these four dimensions. In this section, I will discuss the classification of passive components.

2.2.1 Silicon waveguide

In a submicron SOI platform, the single mode waveguide width is about 2 times larger than the thickness of SOI. Thus the difference of effective index between fundamental TE mode (TE0) and fundamental TM mode (TM0) is huge, showing large birefringence. Usually TE0 mode is the most fundamental mode and is the mode used for light routing in a waveguide.

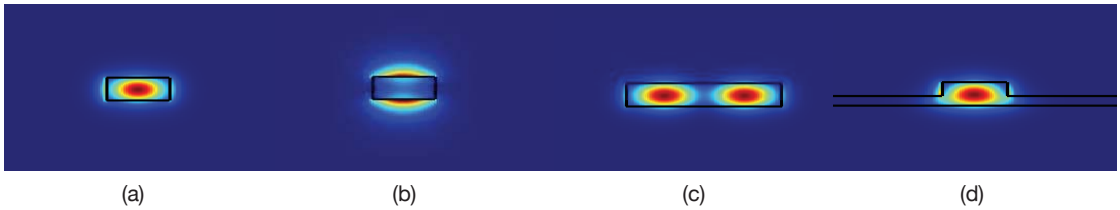

Figure 2-2. Basic silicon waveguides and mode profiles. (a) TE0 mode and (b) TM0 mode of a 500 × 220 nm^2 silicon ridge waveguide. (c) TE1 mode of a 1200 × 220 nm^2 silicon ridge waveguide. (d) TE0 mode of silicon rib waveguide with 500 × 220 nm^2 ridge and 90 nm thick slab. Note that SiO2 surrounds all the waveguides.

Figure 2-2 shows three basic silicon waveguide and basic modes. 500 × 220 nm2 is the most typical single mode waveguide offered by the OpSIS-IME platform. The mode profile of the two most fundamental modes, TE0 and TM0, are plotted in Figure 2-2 (a) and (b), respectively. The effective index at 1550 nm is 2.445 for TE0 and 1.773 for TM0, showing high birefringence. Another typical ridge waveguide geometry is a wider waveguide, which is often used for long distance waveguide routing, with lower loss (about 0.3 dB/cm). The fundamental mode (TE0) profile is similar to that of Figure 2-2 (a). This kind of waveguide also support higher order modes. The TE1 mode profile in a 1200 × 220 nm2 is shown in Figure 2-2 (c) as an

example. Another important type of waveguide is rib waveguide with a ridge in the center, on top of a slab layer. Optical mode is guided in the ridge part. Today's silicon modulators are built on the rib waveguide structure, with the PN junction (or PIN junction) formed at the ridge part and metal contact at the rib part. Compared with the surrounding material SiO2, silicon is more dispersive and temperature sensitive, which should be taken into consideration during design of silicon photonic devices. More detailed information can be found in [50]. Adiabatic waveguide tapers are designed to transit between different types of silicon waveguides, as shown in Figure 2-3.

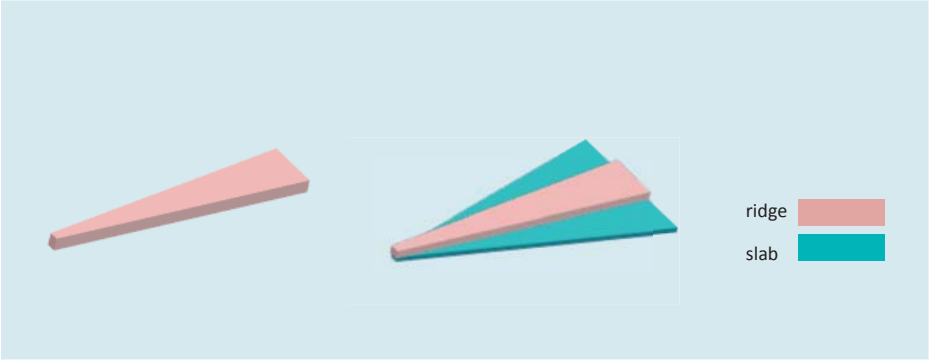

Figure 2-3 Waveguide tapers that enables adiabatic mode transitions between waveguides. (a) Ridge to ridge taper. (b) Ridge to rib taper.

2.2.2 On/off chip couplers

Light can either vertically or horizontally coupled on/off a silicon chip from/to fiber, rendering two kind of couplers: grating coupler (GC) that enables vertical coupling and edge coupler (EC) that enables lateral coupling from the chip facet.

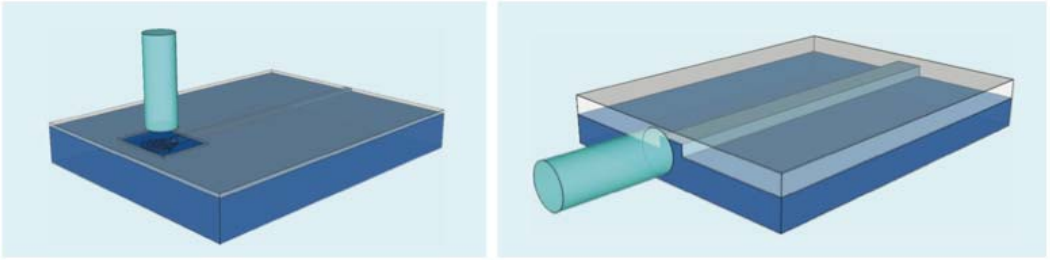

Figure 2-4. (From [25]) On/off chip couplers. (a) Vertical coupling of optical fiber to an on-chip grating coupler. (b) Edge-coupled optical fiber to an on-chip waveguide.

One major advantage of grating coupler is it enables wafer scale testing without dicing the wafer into chips. All the designs, either components or systems, can be tested in wafer scale, which dramatically saves the qualification and testing time. However, grating couplers suffer from low efficiency, wavelength dependency and polarization sensitivity.

Theoretically, the efficiency of GC cannot be higher than –3 dB if the surrounding material (such as SiO_2 in a SOI platform) is symmetric, since light has the equal chance to scatter out of the chip to the fiber or down to the substrate. In order to improve the efficiency, lots of engineering have been proposed and demonstrated to break the symmetry, such as adding a metal reflection layer at bottom of BOX [37], growing extra material layers on top of ridge silicon (polysilicon in [51], germanium in [52]) or using another dielectric layer (such as SiN [38]) on top of ridge silicon.

To address the polarization sensitivity, 2D grating coupler that splits TE and TM modes into two separate paths are proposed. The loss of such grating couplers is high (> 5 dB). While grating coupler enabled commercial SOI platform do exist (for example, the Luxtera platform [37]), grating couplers are more often used in research

and wafer scale characterizations instead of in a real products due to its limitation in insertion loss, bandwidth and polarization sensitivity.

An inverse taper edge coupler can be used to expand the mode size by gradually decreasing confinement factor, thus reducing coupling loss. Such edge couplers also have the advantage of low wavelength dependence. But they have to appear at the edge of the die and are only accessible after wafers are diced. Polishing might be required to get optical quality facet.

Currently, GCs are more often used for device characterization on waer. For most of the silicon photonics products, EC out wins GC since it is polarization insensitive and wavelength insensitive.

2.2.3 Power routing

The on-chip power routing includes power propagating, splitting, crossing and reflecting. One of the most fundamental power-propagating components is of course waveguide. But more generally any on-chip device functions as power propagator since they always guide optical power from one point to another.

In terms of power splitting, a fundamental devices is a 1 × 2 power splitter, which can be realized by a Y-junction or a 1 × 2 multimode interference (MMI) coupler. Another basic power splitting device is 2 × 2 couplers, which can be realized by a 2 × 2 MMI coupler or a directional coupler (DC). 2 × 2 MMI couplers usually functions as 3dB coupler based on the MMI theory [53,54] but DC can realize arbitrary coupling ratio based on the coupled mode theory [55,56]. One can also design 1 × N, N × N, and N× M power splitters based on the MMI theory.

Waveguide crossing has been extensively studied to realize power crossing with minimal scattering loss and crosstalk. The basic theory guiding the design of a

waveguide crossing is also MMI theory (for single level crossing) and coupled mode theory (for multi-level waveguide bridges).

As for on-chip power reflection, distributed Bragg reflector (DBR) and Sagnac loop are two typical structures.

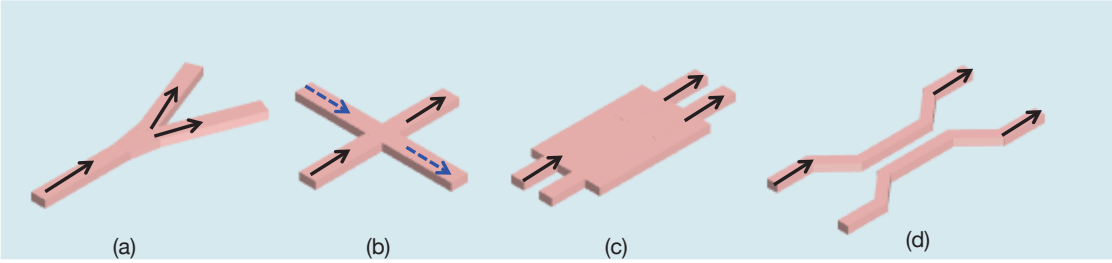

Figure 2-5. Basic power routing devices. (a) Y-junction. (b) Waveguide crossing. (c) 2 × 2 MMI 3dB coupler. (d) Directional coupler.

Geometry of directional couplers and DBRs are usually regulated, leaving limited space in designing. Structures such as Sagnac loops are basically dependent on the 1 × 2 coupler. Although with work experriences on devices such as DCs and 2 × 2 MMI couplers, my research focuses on designing and optimizing Y-junctions and crossings, which will be discussed in Chapter 2.

Figure 2-5 sketches some of the most widely used power routing devices such as Y-junction, crossing, 2 × 2 MMI 3dB coupler and DC.

2.2.4 Wavelength routing

Wavelength routing can be divided into two types: narrow band routing and wide band routing. For narrow band routing, devices such as arrayed waveguide gratings (AWG) [57] and Echelle gratings [58] are important for the wavelength

division multiplexing (WDM) communication networks. Wide band wavelength routing is important for passive optical networks (PON). My research is focused on the later type. I will discuss a novel O-/C-band wavelength diplexer design on SOI platform in Chapter 3.

2.2.5 Polarization handling

Polarization handling involves manipulating of optical modes in waveguides, including polarization splitting, rotating and coupling (for application in mode division multiplexing (MDM) [59]). As been discussed in 2.2.1 , submicron SOI platform suffers large birefringence. However, in a single mode fiber, polarization is not maintained but instead changes randomly with environmental variations, causing random projections of TE and TM to an on-chip waveguide. For low-cost, high-volume applications, being able to deal gracefully with both polarizations is of the essence. A polarization transparent scheme was proposed in 2006 to solve this issue, as shown in Figure 2-1. [60] The kernel of this scheme is a polarization splitter/rotator (PSR). In this work, I will discuss in Chapter 4 a high performance polarization rotator (PR) and a novel symmetrical PSR.

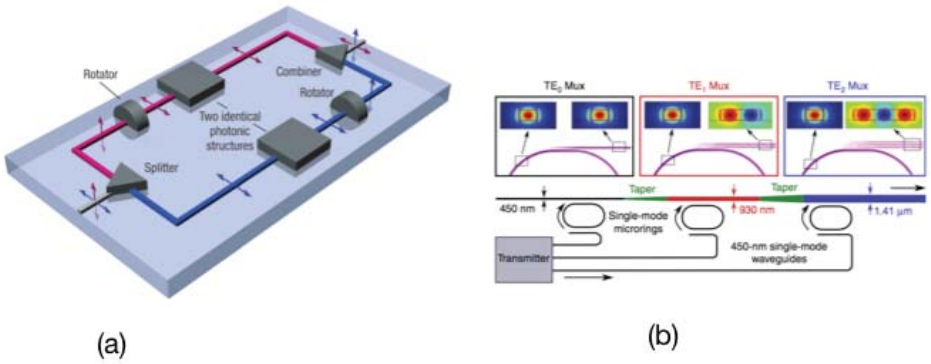

Figure 2-6. (a) (from [60]) Polarization transparent scheme in high confinement waveguides. (b). (from [60]) On-chip MDM scheme.

2.2.6 Phase handling

Phase handling on SOI platform is usually correlated to power handling. For example, the phase difference of 2 × 2 couplers (either MMI or DC) is 90 º. The transfer matrix of a 3dB 2 × 2 coupler can be written as

$$\frac{1}{\sqrt{2}}\begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix}, \tag{2-1}$$

MMI coupler based optical hybrids with 90º and 120º phase difference have been proposed for coherent optical communications. [61,62]

Another phase-related issue is phase uncertainties in silicon waveguides. Due to factors such as fabrication uncertainties, waveguide side wall roughness and thickness variations, the phase in a submicron SOI waveguide is not predictable but varies randomly. A parameter to characterize how well the phase uncertainty is in a waveguide is called coherence length, as discussed in [63]. Thermal phase shifters are often used to actively tune the phases.

2.3 Design Tools And Testing Tools

Since most of the devices involved in this thesis are ultra-compact, finite-difference time-domain (FDTD) method is a good method in simulation. If not otherwise stated individually, the passive components design tools that I use are provided by Lumerical Solutions (https://www.lumerical.com/).

Test structures of the passive components are usually connected with grating couplers, thus cross wafer data can be obtained automatically from our in-house wafer scale test setup (Figure 2-7 (a)). While for active components or systems, edge couplers may be implemented. Thus chip-scale stages (Figure 2-7 (b)) are sometimes built to characterize them.

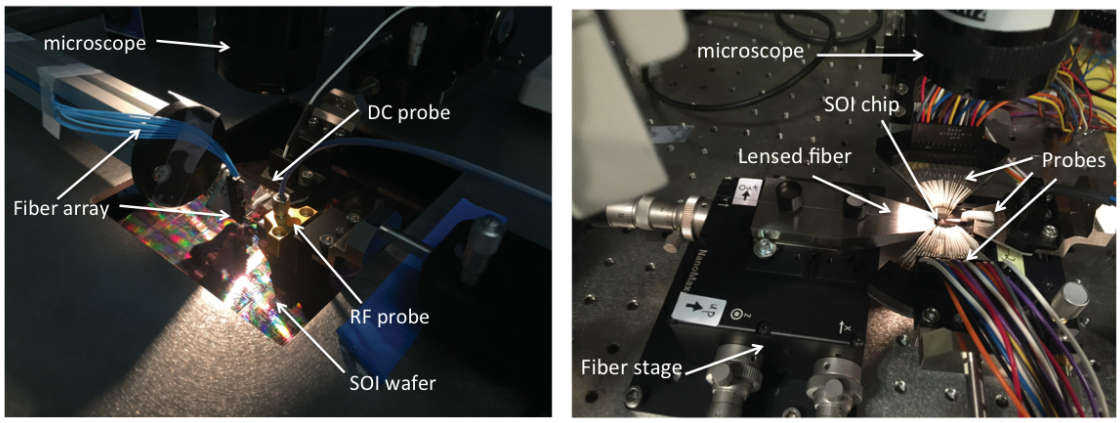

Figure 2-7. (a) Wafer scale test setup with fiber array vertically coupled to grating couplers on-chip. (b). Chip scale test setup with lensed fiber laterally coupled to silicon edge coupler.

Chapter 3

OPTIMIZATION OF FUNDAMENTAL BUILDING BLOCKS

3.1 An Ultralow Loss Waveguide Crossing

3.1.1 The state-of-the-art of silicon waveguide crossing design

Unlike electronic circuits where electrical routing can be accomplished flexibly on multiple layers, optical routing is fundamentally banned from multi-layer integration due to limitations of optical mode coupling and cost control. In order to reach high-volume photonic systems on a single chip, use of the waveguide crossing is unavoidable. It is one of the key building blocks for all silicon photonics platforms. However, directly crossing two waveguides causes severe light scattering, crosstalk and multi-modes-excitation [64]. Prior work has been done to improve crossing performances, based on mode expansion [64–67] , optimized angles [68], multimode interference (MMI) [69–71], Bloch waves [72,73], polymer waveguide bridges [74], sub-wavelength gratings [75], and photonic crystals [76].

Sub-0.2 dB insertion loss and −40 dB crosstalk are the typical performance metrics for the state-of-the-art compact crossings fabricated in SOI CMOS process [65,66,71]. While these crossings have already been integrated into on-chip photonic systems, insertion loss around sub-0.02 dB is greatly desired by the silicon photonics community for use in large-scale integration. Over the past decade, there has been a rapid growth in photonic component count and system complexity of silicon photonic systems [26]. As system size increases, more crossing structures will be required for neat and efficient optical routing and building large scale networks-on-chip (NoC) [77]. Several works have achieved such low loss crossings with different

methods. For example, insertion loss as low as 0.015 dB/crossing was reported in an 8 × 8 silicon optical switch [67], but the taper length of the crossing is about 80 μm to expand the mode size to 6 μm with minimum loss. Such a large crossing is unattractive for large-scale photonic interconnects. In another work, sub-wavelength gratings [75] were explored to reduce the loss to 0.025 dB/crossing but a 0.3 dB taper loss will be introduced when connected to a ridge waveguide. Another approach reported is to design a crossing array instead of a single crossing device with Bloch wave method. Recently, Zhang *et. al.* [73] reported 0.02 dB/crossing loss in a 101 × 101 crossing array fabricated on a 250 nm SOI with electron beam lithography (EBL). However, with the feature size of the Bragg-grating-like subwavelength nanostructure as small as 50 nm, the performance of such a device still remains unknown when transferred into a CMOS photonic process where 193nm or 248nm Deep-UV lithography is typically used. For such crossing arrays, waveguide routing is also intuitively inconvenient when large-scale, high-complex photonic systems are involved. It would be much more routing efficient to lay down a single crossing wherever needed, especially for complex photonic systems.

As one of the most basic building blocks, performance uniformity is definitely an critical performance metric, but few papers report this important metric.

In summary, an ultralow loss single crossing with compact size, stable performance and CMOS process compatibility is greatly desired yet no such crossings with sub-0.02 dB loss had been reported to the best of our knowledge.

In this work I designed and characterized two compact, ultralow loss, single layer, broadband crossings with optimized center wavelength at 1550 nm and 1310 nm, respectively. Cross-wafer average insertion loss of 30 dies (i.e., reticles) is −

0.0278 ± 0.0092 dB/crossing for the device centered at 1550 nm and 0.0168 ± 0.0047 dB/crossing for the 1310 nm device. For both crossings, the device footprint is 9 × 9 μm^2, crosstalk is below −37 dB and wavelength dependence is less than 0.09 dB in a 60 nm range with respect to center wavelength.

3.1.2 Design and fabrication

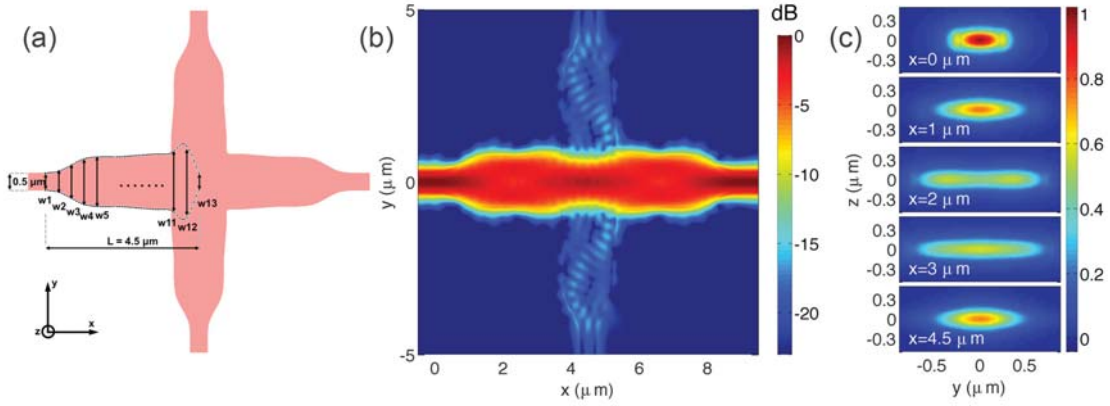

Figure 3-1. (a). Schematic device layout. The device is symmetric and constituted by four identical tapers. The taper is defined by spline interpolation of *w*1 to *w*13. (b) Log-scale Electric field distribution at 1550 nm from FDTD simulation. (c) Mode evolution of the left taper with light input from the left side.

The design methodology in this work was based on our previous report of a low-loss waveguide crossing at 1550 nm [66]. Note that similar crossing design was earlier reported by Sanchis *et. al.* [65] on 250 nm thick top silicon SOI wafer. Our platform offers a 220 nm thick SOI wafer.

Particle swarm optimization (PSO) coupled to the finite-difference time-domain (FDTD) method was utilized to generate the optimal design. This method has

already proved its strong capability in designing compact, multiple-parameter optical devices [34,66]. Schematic layout of the crossing is shown in Figure 3-1(a). It is constituted of four identical tapers respectively orientated at east, west, south and north with a shared center point. The taper length, L, is fixed to 4.5 μm but the width is defined by 13 variables, i.e., $w1$, $w2$, … to $w13$ as indicated in Figure 3-1 (a). These 13 variables are equally distributed along the taper length, with a spacing of 0.375 μm (4.5 μm/ 12). The final device geometry is defined by spline interpolation of the width variables. Four short straight ridge waveguides are appended to the tapers to lead-in/lead-out light. During optimization, $w1$ and $w13$ are fixed as the same as the waveguide width, which is 0.5 μm for the 1550 nm device and 0.42 μm for the 1310 nm device. Note that although it looks from Figure 3-1(a) that w12 has trivial contribution to the final geometry, it is actually as important as other width variables in the very beginning of optimization when one has little idea of what the final result would be. The initial value is set to be the same as waveguide width. As the crossing geometry evolves, w12 naturally increases and merges into the cross-sectional region. The width variables were sometimes manually restricted to achieve smooth structures (wavy structures are usually formed by the nature of multiple-parameter optimization) and pass the design rule check (DRC) required by foundry. These two devices were optimized for TE0 mode.

Optimization figure of merit (FOM) for the crossing is defined as normalized TE0 power transmission minus crosstalk and reflection at a certain wavelength, written as FOM_{λ}. In order to achieve a wavelength insensitive device, we first chose 11 wavelength points across a 100 nm range (centered at 1550 nm and 1310 nm for the different devices, respectively) and take the average of FOM_{λ} as FOM_{avg}.

Maximizing FOM_{avg} dramatically reduces the wavelength sensitivity as well as crosstalk and reflection. The device was then further optimized at the center wavelength. A so-called 2.5D propagator method was first run to quickly reach an approximate optimization state. The 2.5 D propagator first takes in vertical modes of the core waveguide structure of a certain material, over a desired range of wavelengths. Then by calculating the corresponding effective 2D indices, the 2.5D propagator reduces the 3D problem into an effective 2D problem. A 3D FDTD simulation was then introduced to achieve the accurate optimization state. Simulation codes for both methods are commercially available from *Lumerical Solutions*.

In Figure 3-1(b), we show a contour plot of electric field distribution of 1550 nm crossing at 1550 nm. Note that the color bar is in log-scale in order to show the weak scattering and crosstalk field. As can be seen, peak magnitude of E-field in the two crosstalk tapers is ~ − 17 dB. No scattering field with magnitude above − 24 dB can be observed outside the crossing area.

The key issue in a designing waveguide crossing is to converge the mode pattern at the cross-sectional region to minimize light scattering and crosstalk. As can be clearly seen in Figure 3-1(c), mode profiles are first expanded from TE0 mode (x = 0 μm) to TE1-like mode (x = 2 μm) and then converged again as TE0-like mode at the crossing center (x = 4.5 μm). The mode pattern at the center can be regarded as a close replica of the input waveguide mode, which is a typical feature of self-imaging due to multimode interference. The observed crosstalk pattern is also a result of multimode interference. The well-engineered taper helps adiabatically convert TE0 mode into multimode and tailor the modes between the multimode region and the crossing center region to reach the well converged mode pattern at center.

For FDTD simulation, the number of mesh points per wavelength (ppw) is a major consideration for the meshing algorithm. After doing a mesh grid sweep, we found 14 ppw is the optimal value considering the tradeoff between simulation accuracy and time cost. The FOM difference was within 1.1 % compared with 26 ppw mesh grid but simulation speed was more than 6 times faster. The output power of crossing was monitored in y-z plane centered at the waveguide center, with a monitor size of 4 μm × 2 μm. For both 1550 nm and 1310 nm crossing, we tested the influence of monitor positions along the x-axis and found the difference of FOM_λ at the central wavelength was within 0.2%. Particle warm population was set to 20 and 60-70 generations were generally needed to reach a converged FOM.

The length L is crucial for a taper since it determines how efficient the mode conversion can be [78]. Guided modes are not able to fully converted to each other given a short L, as a result light will be scattered instead of keep guided as it propagates along a taper. In our previous work [66], a 3 μm long taper was selected and it turned out the simulated FOM_{1550} saturated at 0.965 (i.e., − 0.154 dB), with experimental device performance of − 0.18 dB. However, the benefit to FOM drops quickly after L exceeds a certain value. Note that in Ref. [67], even for a crossing with $L \sim 80$ μm, the insertion loss, − 0.015 dB, is not much improved from our design. Long L is also undesirable for high-density silicon photonics integration. After several tries, we chose $L = 4.5$ μm as the optimal value. As for the number of width variables, 13 is a moderate number for the crossing with L = 4.5. Fewer width variables would have difficulty defining the crossing geometry while significantly more width variables would not notably improve the FOM but would harm the convergence speed of PSO algorithm.

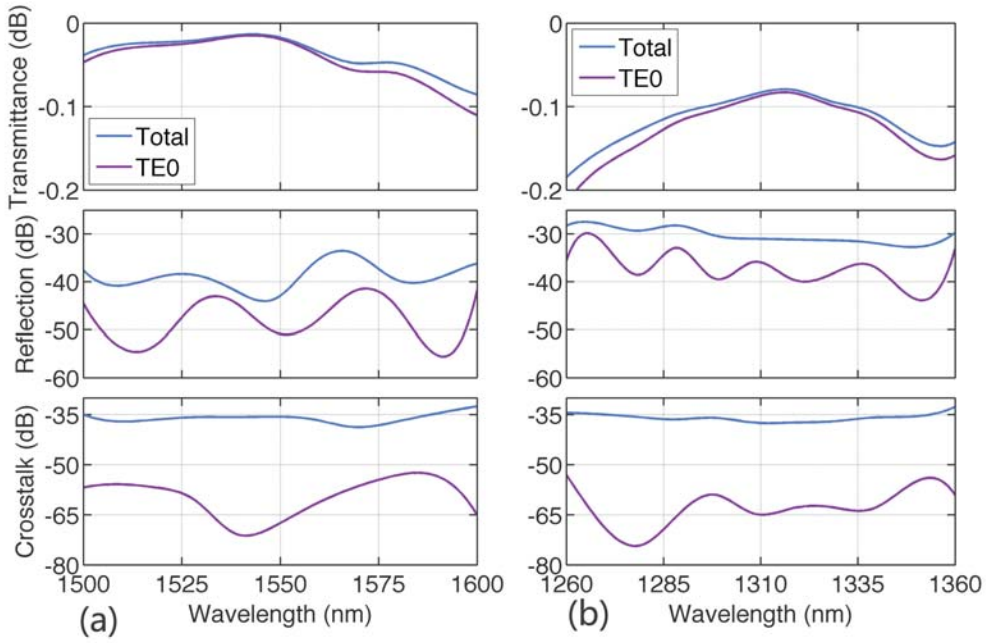

Figure 3-2. Simulated transmittance, reflection and crosstalk of (a) 1550 nm crossing and (b) 1310 nm crossing in a 100 nm range.

Figure 3-2 shows the simulated transmittance, reflection and crosstalk for the 1550 nm device (Figure 3-2 (a)) and 1310 nm device (Figure 3-2 (b)). Curves in blue represent total normalized light power while those in purple mean light power for TE0 mode only. For transmittance, the variation in a 100 nm range is around 0.1 dB for both crossings. It's also clearly shown in the figure that the center wavelengths of 1550 nm and 1310 nm are the most optimized wavelengths. Reflection in Figure 3-2 (a) is slightly better than that in Figure 3-2 (b), but even the maximum total reflection power in Figure 3-2 (b) is relatively small (− 28 dB, i.e., 0.16%). Total crosstalk power is below −33 dB for both crossings in the simulated 100 nm ranges. Crosstalk of TE0 mode is even one times smaller, well below − 50 dB. In a word, simulation

results in Figure 3-2 demonstrated two low-loss, low-crosstalk and broadband single layer waveguide crossings centered at 1550 nm and 1310 nm respectively. The detailed crossing geometry parameters are provided in Table 3-1.

Table 3-1. Crossing geometry parameters (μm)

ID	L	*w*1	*w*2	*w*3	*w*4	*w*5	*w*6	*w*7	*w*8	*w*9	*w*10	*w*11	*w*12	*w*13
1550	4.5	0.5	0.6	0.95	1.32	1.44	1.46	1.466	1.52	1.58	1.62	1.76	2.15	0.5
1310	4.5	0.42	0.78	1.2	1.312	1.316	1.338	1.423	1.466	1.585	1.726	1.99	2.00	0.42

It's worth pointing out that the crossings are insensitive to the SOI silicon thickness and thus highly applicable to other SOI platforms. For example, with the same x-y plane geometries reported in this work, 3D FDTD simulation showed very good FOM: $FOM_{1550} = 0.984$ (i.e., − 0.070 dB) and $FOM_{1310} = 0.954$ (i.e., − 0.205 dB) for 250 nm thick silicon and $FOM_{1550} = 0.962$ (i.e., − 0.168 dB) and $FOM_{1310} = 0.935$ (i.e., − 0.292 dB) for 300nm thick silicon. One can expect further improvement by further optimizing the crossings on these SOI platforms.

3.1.3 Measurement and discussion

Devices were fabricated using a CMOS-compatible process on an 8-inch SOI wafer at the Institute of Microelectronics (IME)/A*STAR through an OpSIS multi-project-wafer run. The top silicon thickness is 220 nm, on top of 2 μm buried oxide (BOX). Devices were patterned by 248 nm deep UV photolithography, followed by dry etching. The top silicon was completely removed outside the crossing area, left with a 220 nm thick single layer device. Tiles were used around the devices with reasonable distances away to achieve a certain filling ratio. Finally a 2.3 μm oxide-cladding layer was deposited on top of the silicon layer.

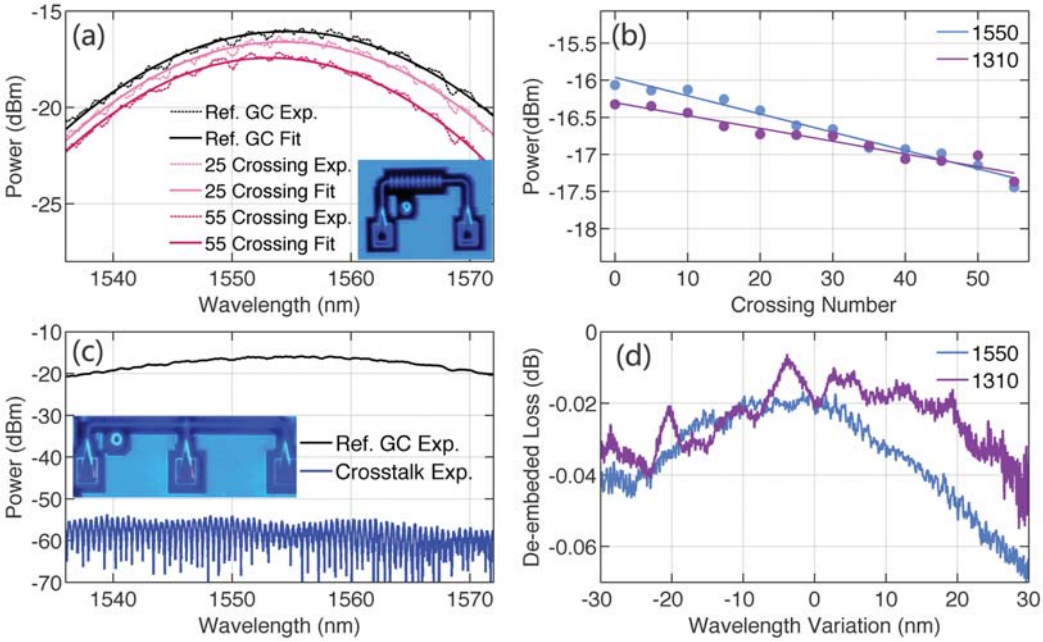

Figure 3-3. Device performance characterization. (a) Experimental (dot curve) and fit (solid curve) spectra at different cascaded 1550 nm crossings. Inset is a fabricated test structure with 10-cascaded crossings. (b) Peak power (dots) extracted from measured spectra for 1550 nm crossing (blue) and 1310 nm crossing (purple). The slope from linear fitting of peak powers represents insertion loss per device. (c). Experimental spectra of reference GC loop (black) and crosstalk (blue). Inset is fabricated crosstalk test structure. (d) Insertion loss variation in a 60 nm range after de-embeding the spectrum of the reference GC loop.

Testing farms with gradually increased number of cascaded crossings were utilized to extract insertion loss. A three terminal structure with grating coupler (GC) connected was used to characterize the crosstalk by measuring spectrum of any two adjacent GCs. GCs that vertically coupled light on and off chip enabled the cross-wafer measurement. The pitch of two adjacent grating couplers is 127 μm, determined by the pitch of the fiber array. A clear layout and fabricated micrograph of the grating

coupler design was shown in [79]. The GC is designed to support TE0 mode, which is also the mode that our crossings optimized to work for. The die size on the wafer is 2.5 cm × 3.2 cm, splitting the 8-inch wafer into 31 dies. Excluding one incomplete die, a total of 30 dies were tested. An Agilent 81600B tunable laser was used as the laser source.

Figure 3-3(a) shows a small sample of measured experimental spectra (dot curves) of the 1550 nm crossing with 0, 25, and 55 crossings. Note that crossing number = 0 also means the reference GC loop, i.e., two GCs routed by a U-turn waveguide. The GC loop introduces a baseline loss of about − 16 dB at its peak, independent to crossing loss. It's worth noticing that the spectra are not notably deformed as crossing number increased, even up to 55 crossings. This indicates that although higher order modes are excited inside the crossing tapers, as we discussed earlier in Figure 3-1(c), an insignificant multi-modal power reaches the output. Almost all the high order modes converted back to TE0 mode by the output point. In this way, mode pattern and light energy are nearly fully conserved. This is an important merit for a highly qualified crossing and is extremely desirable for large scale optical interconnects.

We then fitted each measured spectrum with parabola (solid curves in Figure 3-1 (a)) in a 40 nm range centered at its peak wavelength. The micrograph of fabricated cascaded crossing structure is shown in inset of Figure 3-1(a). The fitted peak powers, shown in Figure 3-1 (b), were then utilized to extract the insertion loss of each crossing in dB/crossing. Blue dots stand for 1550 centered crossing while purple ones stands for the 1310 nm device. The insertion loss obtained from linear fitting in Figure 3-1 (b) is − 0.0246 dB for the 1550 nm crossing, almost an order of magnitude

lower than typical crossing loss fabricated in CMOS process. The 1310 nm crossing surprisingly has an even lower loss, − 0.0173 dB, due to fabrication proximity effect, better than simulation results.

Crosstalk spectrum (the blue curves) of 1550 nm crossing is shown in Figure 3-1 (c), measured from the left two adjacent GCs as in inset of Figure 3-1 (c). The crosstalk is not wavelength sensitive and measured to about − 37 dB, low enough for practical applications. For 1310 nm device, similar results were observed. Note that the crosstalk signals lies at the border of the noise floor of our testing system. Real crosstalk should be even smaller than this value.

By de-embedding the reference GC spectrum, we were able to get the pure wavelength-dependent crossing spectrum. For both designs, we chose the spectrum of 55-cascaded crossings – largest number in our layout – to do de-embed since device flaws will be accumulated but random factors will be suppressed as device number increases. De-embedded results were then divided by crossing number 55, to show the performance of a single device, as presented in Figure 3-1 (d). In a 60 nm range, the variation of 1550 nm crossing is as low as 0.05 dB with smooth spectrum. For the 1310 nm device, the variation is about 0.035 dB with some small ripples. The ripples indicate that some optical modes other than TE0 mode come out of the crossing. However, the ripple magnitude is within 0.012 dB, which is still negligible for most applications. An optical micrograph with cascaded crossings is plotted in Figure 3-4.

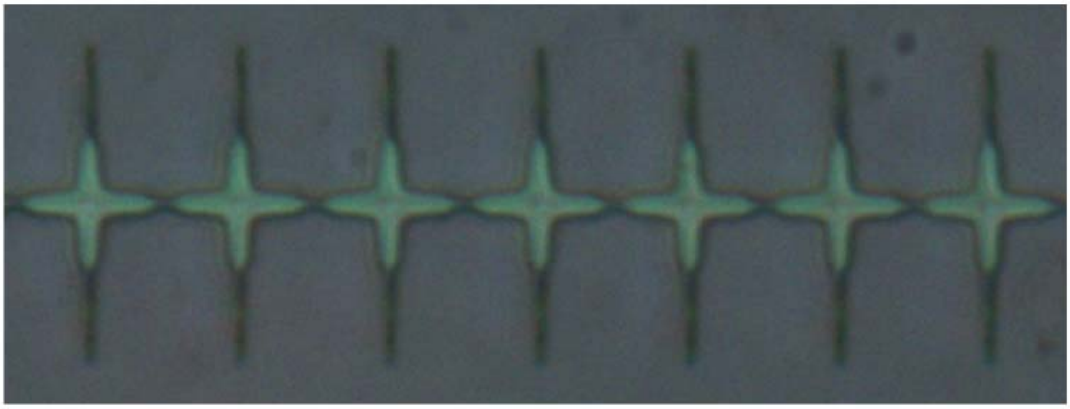

Figure 3-4. Optical micrograph of cascaded waveguide crossings.

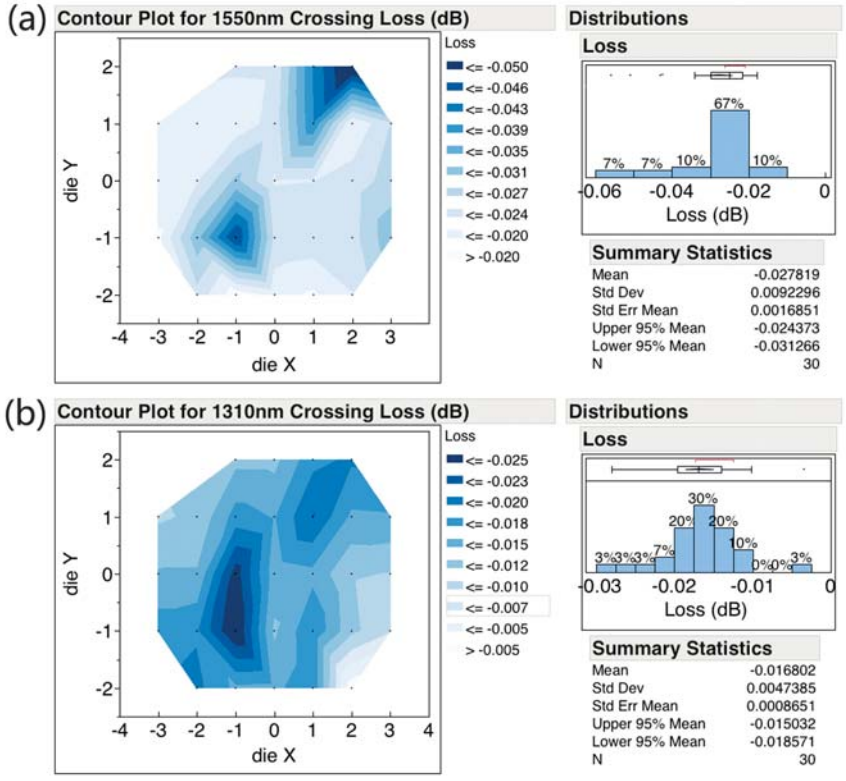

Figure 3-5. Cross-wafer measurement. Contour plot (left part) and histogram analysis (right part) of insertion loss distribution for (a) 1550 nm crossing and (b) 1310 nm crossing.

Performance uniformity is an important metric for any device aimed for system applications, especially for devices that act as basic building blocks in silicon photonics, such as grating couplers, y-junctions and crossings. The deviation of performance can be from either the SOI wafer itself, such as thickness variation of top silicon, or the fabrication process flow deviation on each die.

We performed cross-wafer measurement for insertion loss on 30 dies. Statistical analysis is summarized in Figure 3-5. The contour plot clearly shows the performance variation across the wafer for each crossing. The histogram on the right shows the loss distribution in terms of dB. As can be seen, the distribution more or less appears Gaussian for both devices. For the 1550 nm crossing, we calculate that the loss is − 0.0278 ± 0.0092 dB/crossing, bounded between − 0.0559 and − 0.0178 dB. The 1310 nm device loss is − 0.0168 ± 0.0047 dB/crossing, bounded between − 0.034 dB and − 0.0028 dB.

Cross-wafer wavelength variation was calculated as in Figure 3-5(d). The result is 0.072 ± 0.022 dB for 1550 nm crossing in a 60 nm range. The variation for 1310 nm crossing is 0.087 ± 0.027 dB. Crosstalk was measured on five dies – (0, 0), (-2, 0), (2, 0), (0, -2), (0, 2), which are evenly distributed across the wafer. All crosstalk spectra were found at noise floor. The crosstalk from five-die analysis is bounded between −40 and −35.6 dB with an average of −37.5 dB for 1550nm-centered crossing. For 1310nm crossing, the upper bound of the crosstalk value is between −34.1 and −43.6 dB with an average of 37.5 dB. Real crosstalk is likely to be even lower.

The above cross-wafer analysis confirmed that the two crossings demonstrated in this work are fabrication insensitive, making them reliable component of a complex

integrated photonic system. Taking 1550 nm crossing for example, a system containing 50 × 50 mapped crossings already have the ability to include 2500 other devices and yet the maximum loss contributed from crossing is estimated to only − 1.39 dB (− 0.0278 dB × 50). Assuming all input light sources are identical in such a system, the maximum crosstalk is still about -20 dB or less (smaller than 1 % of the input light) after being enhanced 50 times (i.e., increased about 17 dB). Moreover, a pure 50 × 50 crossing matrix only consumes an area of 500 × 500 μm2 (including 1 μm long adjunct waveguide for each crossing), still small compared with current integrated photonic systems. Therefore, with these two crossings, integrated photonics designers can almost intersect waveguides freely to a very large scale, without worrying about energy loss, crosstalk and higher order mode interference.

3.1.4 Optical proximity correction

The cross-wafer loss variation is relatively low considering the wafer thickness variation and fabrication proximity effect at 248 nm wavelength. However, optical proximity correction (OPC) [80], which is used in microelectronics industry as a resolution enhancement technology (RET), if applied to silicon photonics, can help making photonic device geometry more predictable and thus further improve the performance as well as stability for a lot of geometry sensitive photonic devices [81,82]. This technique is expected to be important for future work in this area. Despite data not currently available for these two specific crossings, evidence has been observed in a different crossing design on the same wafer. The crossing mask was engineered with OPC. Analysis data on five dies showed that the insertion loss improved from − 0.506 ± 0.133 dB/crossing to − 0.184 ± 0.012 dB/crossing, which is closer to the simulation result. For this crossing, OPC not only improved performance,

but also decreased the standard deviation, indicating more uniformly fabricated geometries across the wafer.

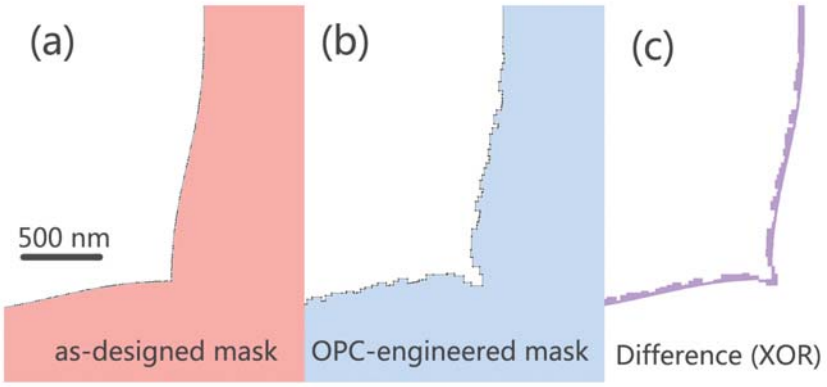

Figure 3-6. Schematic layout of the junction part of crossing mask. (a) Mask as designed. (b) Mask with OPC engineering. (c). Symmetric difference (XOR) of layout (a) and (b).

We taped out a control group to study the function of optical proximity correction (OPC) on crossing. Note that the crossing involved for OPC is a different device from what we reported in the main manuscript. The insertion loss of this crossing is -0.27 dB from 3D FDTD simulation. The junction part of the crossing mask is schematically shown in Figure 3-6. Figure 3-6 (a) represents the as-designed mask, i.e., the mask sent to foundry is the same as design, which is the case for almost all the current silicon photonics designs. Figure 3-6(b) shows the OPC-engineered mask with re-gridded edge from Figure 3-6(a), generated from a commercial software tool, *Calibre Workbench* from *Mentor Graphics,* which is initially designed for microelectronics. Curved device edges are common in silicon photonics community but are quite unusual for microelectronics industry. Thus the curved edges in Figure

3-6(a) were first ‘De-angled’ to orthogonal edges only, i.e., the angles of polygon nodes are restricted to 45, 90, 145 and 180 degrees. The maximum distance for the ‘De-angle’ operation was set to 10 nm to avoid introducing unwanted corrugations of waveguide edge. OPC was then performed on the ‘De-angled’ structure, generating OPC-engineered mask as shown in Figure 3-6 (b). The mask difference between Figure 3-6 (a) and Figure 3-6 (b) is shown in Figure 3-6 (c).

We show in Figure 3-7(a) and (b) measured spectra (dot curves) of the fabricated crossings (data was from the same die of the wafer) with respect to the control group of crossing masks shown in Figure 3-7(a) and (b). The crosstalk (bottom part of the figures) of this control group doesn’t differ much – both at noise floor with crosstalk lower than -37 dB. However, insertion losses behave quite differently. Figure 3-7(a) shows transmission spectra (top part of the figure) of as-designed crossing with 0, 8 and 16-cascaded crossings while Figure 3-7 (b) also shows the same set of spectra of the OPC-engineered crossing.

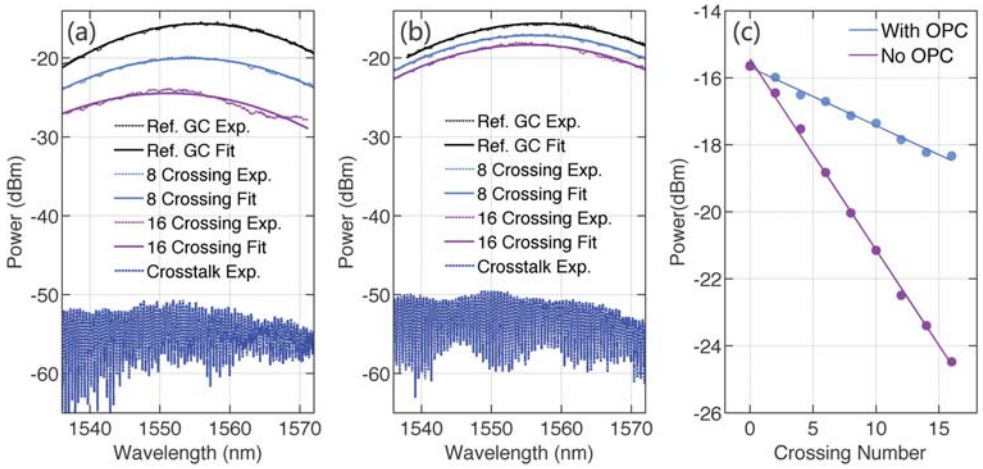

Figure 3-7. Crossing performance comparison. (a) Spectra of the crossing without OPC. (b) Spectra of the crossing with OPC. (c) Peak power (dots) extracted from measured spectra for insertion loss (i.e., slope of linear fitting) characterization.

As clearly seen, spectra in Figure 3-7 (b) drops much slower than that of Figure 3-7 (a) as crossing number increases, indicating lower insertion loss. Also the spectrum of 16-cascaded OPC-engineered crossings (purple dot curve) are not notably deformed in Figure 3-7 (b), but the comparison spectrum in Figure 3-6(a) is already deformed from a normal parabolic shape (which is introduced by grating coupler (GC) in the measurement loop, indicated in the main manuscript) due to high order mode excitation and accumulation effect. The insertion loss spectra of Figure 3-7 (a) and Figure 3-7 (b) was fitted by parabola (solid curves in these two figures) in a 40 nm range centered at its peak wavelength. The fitted peak power was depicted in Figure 3-7 (c) (dots) to extract insertion loss by linear fitting. The slope of the linear fittings gives insertion loss in dB/crossing. The insertion loss of as-designed crossing (purple) is fitted to be − 0.57 dB/crossing but for the OPC-engineered crossing, loss improved a lot, − 0.173 dB/crossing, more than two times smaller.

Further analysis on five dies that evenly distributed on the wafer confirmed the consistency of fabrication. For the as-designed crossing, the calculated loss is -0.506 ± 0.133 dB/crossing, bounded between − 0.575 and − 0.307 dB. The OPC-engineered device loss is − 0.184 ± 0.012 dB/crossing, bounded between − 0.201 dB and − 0.174 dB. The results demonstrated the great function of OPC in improving crossing performance as well as performance uniformity. Thus it's expected to further improve the performances such as cross-wafer uniformity of the ultralow low crossings reported in the main manuscript.

From above analysis and existing reports [81,82], it is believed that the OPC technique, a technique initially designed to serve microelectronics, is also generally applicable to geometry sensitive photonic devices such as crossings, distributed Bragg reflectors (DBR), photonic crystals, etc. Note that The OPC model was built from the source parameters provided by the fab. In future, experimental data from specific test structures will be gathered to build a more concrete and precise OPC model that should help improve fabrication stability and predict device performance.

3.2 An Ultralow Loss Y-Junction

3.2.1 Introduction

As one the most basic building blocks, a low loss and compact Y-junction is critical to silicon photonic circuits. A Y-junction formed by circular bends with a butt waveguide in between to avoid the sharp corners is observed to have over 1 dB insertion loss in our experiment. Mach-Zehnder modulators consisting two such Y-branches readily have more than 2 dB insertion loss in the budget, regardless of other losses from free carrier absorption and on-and-off chip light

coupling, making them less competitive than state of the art III-V electro-optic modulators, which usually have around 5 dB fiber to fiber insertion loss. Obviously, complex and large scale integrated optical circuits cannot be built on such lossy components. Moreover, the abrupt waveguide discontinuity causes light scattering and back-reflection. Implicit resonant cavities formed by these scattering sites degrade the system spectral response.

The Y-junction design in this work is based on a previous reported design from our group. [34] In that design 0.28 +/– 0.02 dB insertion loss was achieved from crosswafer measurement. Here I show a new version with 0.07 +/– 0.04 dB insertion loss, improved by a factor of 4.

3.2.2 Design and simulation

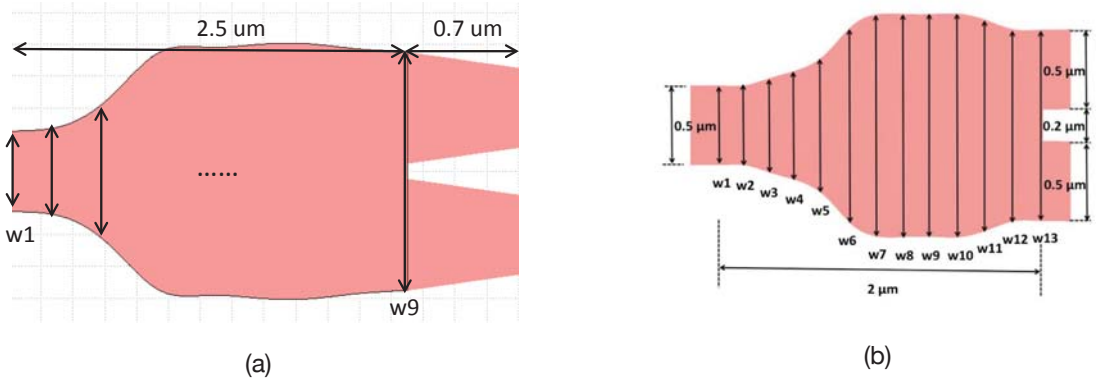

Figure 3-8. Y-junction design schematics (not to scale). (a) New Y-junction design. (b). Old Y-junction schematic from [34] as a reference.

Figure 3-8 (a) shows the schematics of the Y-junction. Figure 3-8 (b) shows the schematics of the old Y-junction as a reference. The device length of the junction

part is set to be 2.5 μm, slightly increased from 2μm as in the old version. Similar to the work in waveguide crossing (chapter 3.1), the junction part is digitalized into 8 segments. However, instead of directly collecting the optical power with two single mode waveguide bends at the end of waveguide junction, I added a short taper in between. It turned out even this small change can be of great improvement.

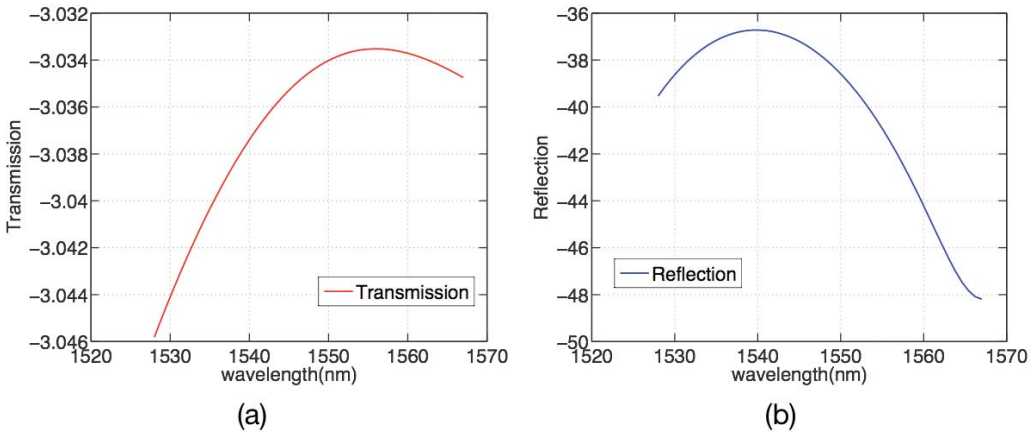

Figure 3-9. Simulated transmission (a) and reflection (b) in dB scale.

PSO coupled FDTD simulation was then performed on the Y-junction. The simulated efficiency is higher than 98.9 % (0.048 dB loss) across C-band (Figure 3-9 (a)) and reflection is as low as -36 dB (Figure 3-9 (b)). The E-field is plot in Figure 3-10, showing extremely good balance and no visible scattering loss.

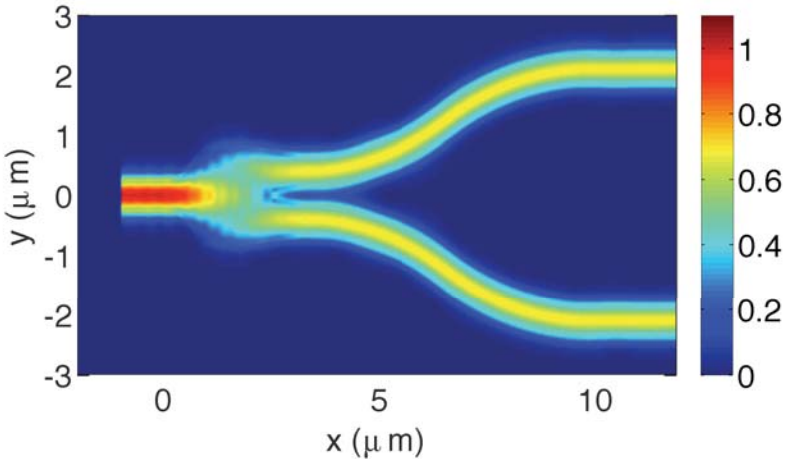

Figure 3-10. Contour plot of electric field distribution at 1550 nm from FDTD simulation.

3.2.3 Measurement

Measurement was done on the wafer scale test setup. Butt-coupled Y-junction pairs (inset of Figure 3-11 (a)) were laid down to accurately extract the insertion loss. Note these pairs are connected to grating coupler loops to enable wafer scale measurement. A sample set of spectra is shown in Figure 3-11 (a). By fitting the spectra in and extracting the peak fiting power, I measured the insertion loss to be as low as 0.06 dB, shown in Figure 3-11 (b). As a fundamental building block in PIC, uniformity is of essential. Crosswafer measurement shows very good die-to-die uniformity. The overall acrosswafer performance is 0.07 +/– 0.04 dB from 25 dies. A contour plot is shown in Figure 3-11 (c). By comparing to state of the art Y-junction or 1×2 MMI splitter designs (Xiao 2013 [35]; Zhang 2013 [34]; Pang 2012 [83]; Van Thourhout 2006 [84]), our design is outstanding in insertion loss with comparable device footprint, as clearly shown in Figure 3-11 (d).

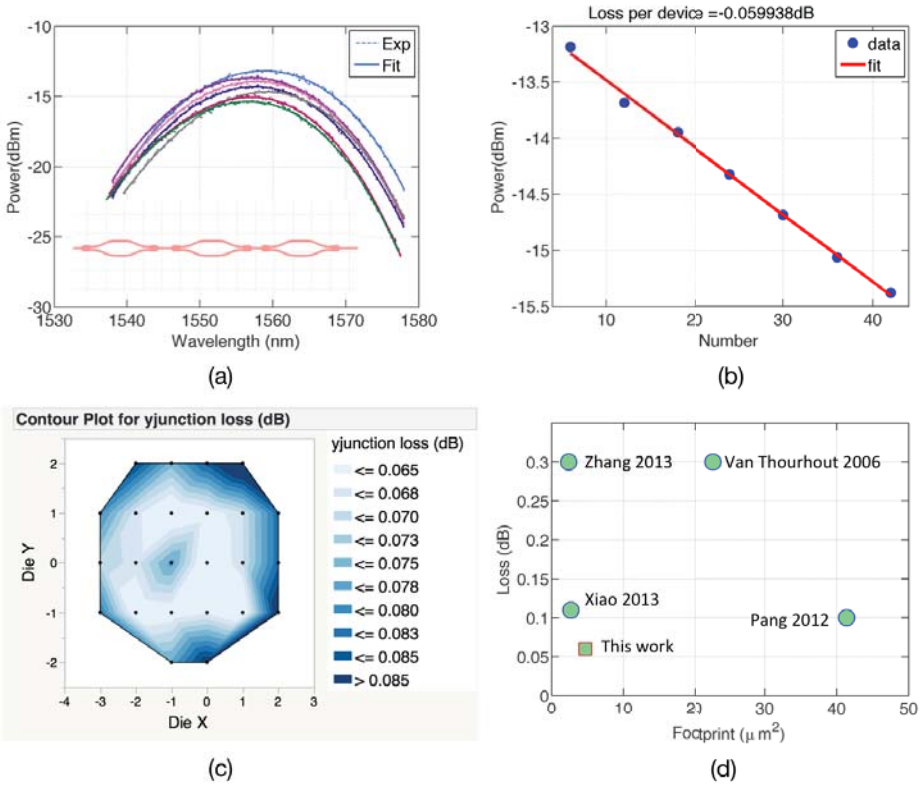

Figure 3-11. (a) Experimental and fitted spectra with a set of butt-coupled Y-junction pairs (with schematic layout shown in the inset). (b) Insertion loss from linear extraction. (c) Measured crosswafer performance. (d) A comparison to the state-of-the-art.

Chapter 4

OPTIMIZATION OF APPLICATION-SPECIFIED COMPONENTS

4.1 A Novel Bent Taper Concept

The community of integrated optics almost takes it as a convention that a taper is ought to be linear, such as edge coupler taper, bi-layer mode convertor taper. Yet another conventional is to use single mode waveguide for waveguide bending, to avoid multimode mixing. However, what if we consider a "worst" combination of these two: a bent taper that is multimode? It can actually be very desirable if one can control its behavior by carefully engineering its geometry. In this section, I will propose a novel taper concept in integrated optics, which I refer to it as a "bent taper". I will then present two novel designs that are enabled by this "bent taper" concept in the next two sections: a O-/C-band wavelength diplexer and an ultra-compact polarization rotator.

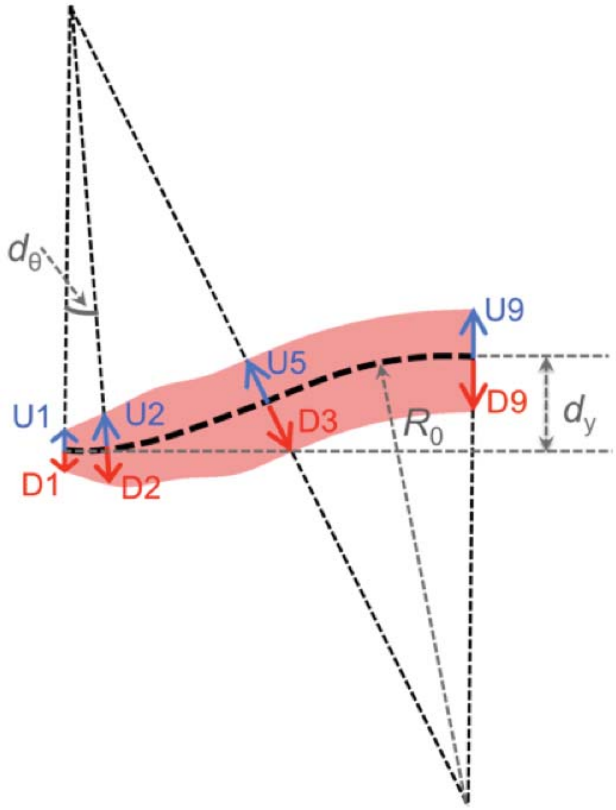

Figure 4-1. Schematic of bent taper.

The schematic of the bent taper is defined in Figure 4-1. The bent taper starts with a typical S-bend. Universally, an S-bend waveguide can be defined by three factors: center radius R_0, vertical offset *dy*, and waveguide width. Instead of fixing the waveguide width as a constant, we choose to vary it at different angles. By changing the bend width along with its angle, a bent taper can be formed. The behavior of a multimode bend is defined by its geometry. If one can control the behavior of a multimode bend, one can achieve more functions than a single mode bend by utilizing the multimode region.

In the example given in Figure 4-1, I discrete the S-bend into 9 segments of equal angles, d_θ, and do interpolation between each segments to make the transition of geometry smooth. Instead of defining symmetric S-bend (now relative to the center radius R_0), we now choose asymmetric geometry for the S-bend to increase the optimization freedom. The center radius R_0 divides the S-bend into two sides: the up side and the down side. Therefore, we have two set of independent width parameters: U1, U2, U3, ..., U9} and {D1, D2, D3, ..., D9}, as indicated in Figure 4-1.

4.2 Novel O-/C-Band Wavelength Diplexer

4.2.1 Motivation

Silicon photonics has great potential for integration in fiber communication systems with the potential to further reduce costs. The O-band and C-band are of interest for any fiber-based transmission due to the low loss of glass in those bands. But commercially, operation in both bands on a single fiber is chiefly found in passive optical networks (PON) for fiber-to-the-X (FTTX) applications (where X can be "home," "building," "curb," etc.). Many C-band designs for integrated, silicon-on-insulator (SOI) optical components have been demonstrated, including all kinds of basic passive building blocks [34,36,57,85,86], high-speed modulators [6,8] and photodetectors [17,18]. Hybrid evanescent coupled lasers [20] as well as silicon external cavity lasers [22] have also been developed for system integration. Although O-band designs are less frequently reported [9,87,88], there is no inherent obstacle to extending C-band designs to the O-band on the SOI platform. However to integrate PON optics, an integrable high-performance SOI wavelength diplexer that can combine/split these two bands is desperately needed.

In previous work, three typical structures are involved in the design of an SOI O/C band diplexer: diffractive grating coupler, a resonator-based structure and a multimode interference (MMI) coupler. Grating-coupler based diplexer designs were reported [89,90] but the insertion loss is high, 2.6 dB in Ref. [89] and 5 dB in Ref. [90]. Another drawback of this structure is that it is designed for coupling light on/off chip, it cannot deal with an on-chip interconnect. A silicon microring-resonator based diplexer was reported for a PON optical network unit (ONU) [91]. The insertion loss for such a design is small but the bandwidth is limited. Different ring geometries are required to deal with different wavelengths across a band. Extra control systems are needed since silicon microrings are quite temperature sensitive. These two factors limit the microring diplexer designs from practical PON applications. Alternatively, MMI-coupler-based diplexer designs have relatively low insertion loss and wide bandwidth. But the footprint usually exceeds hundreds of microns from the results reported in both SOI and III-V materials [92–94]. Currently a truly passive, low-loss, broadband integrated diplexer design with compact footprint and good fabrication tolerance is needed.

In this work, I proposed a novel SOI diplexer design for O-/C-band wavelength multiplex/de-multiplex applications. The fundamental principle of the proposed device is based on the design of the MMI coupler. This device is very efficient, wideband, ultra-compact and fabrication tolerant. Efficiency higher than 94.4% (i.e., insertion loss < 0.25 dB) is achieved for both bands from 3D finite difference time domain (FDTD) simulation with a device less than 15 μm long. The 1-dB bandwidth is about 100 nm. Yield analysis shows a fabrication tolerance of ± 20 nm deviation in the critical dimensions.

4.2.2 Design and optimization

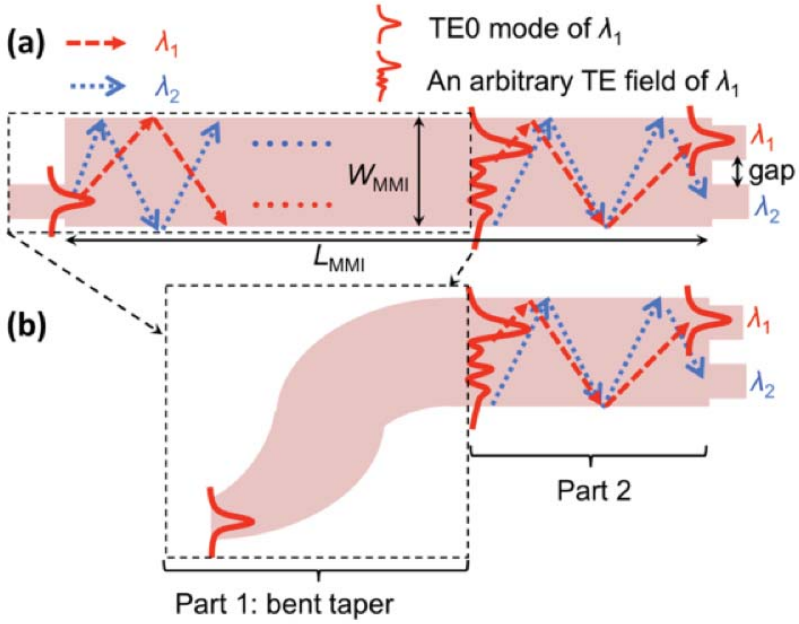

Figure 4-2. (a) Schematic of a conventional MMI-based diplexer. (b) Schematic of a novel MMI-based diplexer using a combined bent taper and multimode waveguide.

The fundamental operating principle of a conventional MMI diplexer is the self-imaging effect; one or multiple images of the input field profile is periodically reproduced as the light propagates along a multimode waveguide region [53]. This effect has been widely applied to designing $M \times N$ couplers, such as coherent hybrid mixers (2 × 2, 2 × 4, 4 × 4 MMI coupler) [86,95]. Furthermore, due to geometry dispersion of the waveguide (i.e., the effective index, n_{eff}, is a function of waveguide width), the self-imaging spots in the coupler deviate laterally for different wavelengths. As a result, a 2 × 2 MMI can achieve wavelength diplexing, as illustrated in Figure 4-2(a).

Without loss of generality, both wavelengths, λ_1 and λ_2, are launched into the lower left port in Figure 4-2 (a). Note that for real applications, two wavelengths may travel contra-directionally but the performance is guaranteed by the reciprocity of a two port passive optical system. In conventional 2 × 2 MMI diplexer design where a multimode straight waveguide is applied, the length of MMI, L_{MMI}, must satisfy the following mode matching condition [94] in order to efficiently split two wavelengths:

$$L_{MMI} = pL_{\pi}(\lambda_1) = (p+q)L_{\pi}(\lambda_2), \tag{4-1}$$

where p is a positive integer, q is an odd integer (usually set to 1), and

$$L_{\pi}(\lambda) = \frac{\lambda}{2\left(n_{eff0} - n_{eff1}\right)}, \tag{4-2}$$

is the beat length of two lowest modes at wavelength λ. n_{eff0} and n_{eff1} are the effective index of these two modes. To slightly relax the mode matching condition and to improve splitting efficiency of the targeted peak wavelengths, an asymmetric structure is usually introduced at the output side of diplexer (right side in Figure 4-2 (a)). [92,93]

A different way to reduce L_{MMI} is to consider the reciprocal property of a passive silicon photonic device. The middle of Figure 4-2 (a) indicates an arbitrary intermediate E-field of the MMI when launching TE0 field at the left side. If one can initially launch an exactly same field profile at the same spot to the MMI coupler, one can imagine that same output profile can be obtained. But the device working distance is greatly reduced now since the MMI effectively starts working from the middle.

Following this idea, here we introduce a novel design to realize both a highly efficient wavelength separation and ultra-compact device size. The schematic is shown in Figure 4-2 (b). The device can be divided into two seamlessly jointed parts:

Part 1: An asymmetric S-bend like taper that adiabatically transits from single mode region to multimode region. We refer to it as a bent taper. The bent taper is used to excite a well-defined initial field profile as indicated in Figure 4-2 (b).

Part 2: A symmetric MMI region. The MMI geometry is engineered with particle swarm optimization (PSO), similar to the ones reported to realize highly efficient Y-junction and waveguide crossing [34,36]. We refer to it as a PSO MMI.

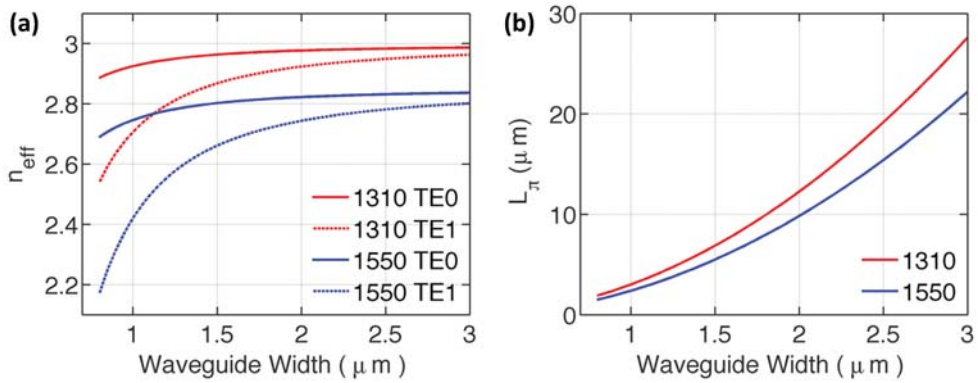

Figure 4-3. (a) n_{eff} v.s. waveguide width (b) Beat length L_π v.s. waveguide width

The first advantage of this design is the compact device size. Compact device size calls for small beat length Lπ(λ) as well as p, q numbers from Eq. (4-1). And from Figure 4-2, one finds small Lπ(λ) requires large effective index difference between the lowest two modes, i.e., [neff0(λ) − neff1(λ)]. From calculations of the effective index versus waveguide width, shown in Figure 4-3(a), [neff0(λ) − neff1(λ)] decreases dramatically as waveguide width increases from single mode region to multi-mode region. The material here is chose to be 220 nm Si on 2 μm buried oxide (BOX). The top cladding is also SiO2. A similar relationship applies to other SOI thicknesses. The

resulting beat length is depicted in Figure 4-3(b). At a 3 μm wide region, Lπ (1550) ≈ 22 μm, which is about 10 times larger than that of a 1 μm-wide region. Similar results can be obtained at 1310 nm. Small waveguide width, WMMI, is chosen for Part 2 of Figure 4-2(b), in order to shrink the footprint of the MMI coupler-based diplexer.

As observed from Figure 4-3(a), $[n_{eff0}(\lambda) - n_{eff1}(\lambda)]$ is more sensitive to the change of waveguide width at smaller widths, which means a narrower MMI coupler is less tolerant of fabrication variation. In order to keep the design within a decent fabrication tolerance regime, the device length must be short if we choose small W_{MMI}. Since q is usually set to 1, p must be small. But p cannot be easily controlled in a conventional geometry like Figure 4-2(a). To relax the rigorous restraint of p value, we introduce a bent taper (Part 1) before the MMI (Part 2), as shown in Figure 4-2(b). The bent taper here, like a short non-adiabatic linear taper, serves as a multimode excitation tool to provide an initial field profile to Part 2. The multimode excitation can happen in a very short distance. However, different from linear tapers, bent taper is asymmetric and has more complicated geometry, thus offers us more freedom to engineer the multimode mixing for different wavelengths. Regardless of bent taper or MMI, any field profile in a multimode waveguide is a superposition of the supported eigenmodes of the waveguide. In this sense, a well-engineered bent taper can thus provide a well-defined initial field (more complicated than a TE0 profile) for the MMI to reduce the its working distance. By introducing the bent-taper, the device length can be reduced and hence, the fabrication tolerance is increased.

Another feature of this design is the high efficiency. A narrower MMI usually has more scattering loss and crosstalk at the output ports due to that fact that the E-field is less confined and separated. We use a PSO MMI coupler in Part 2 instead of a

conventional straight MMI coupler to optimize the device performance after cascading the bent taper with a PSO MMI coupler.

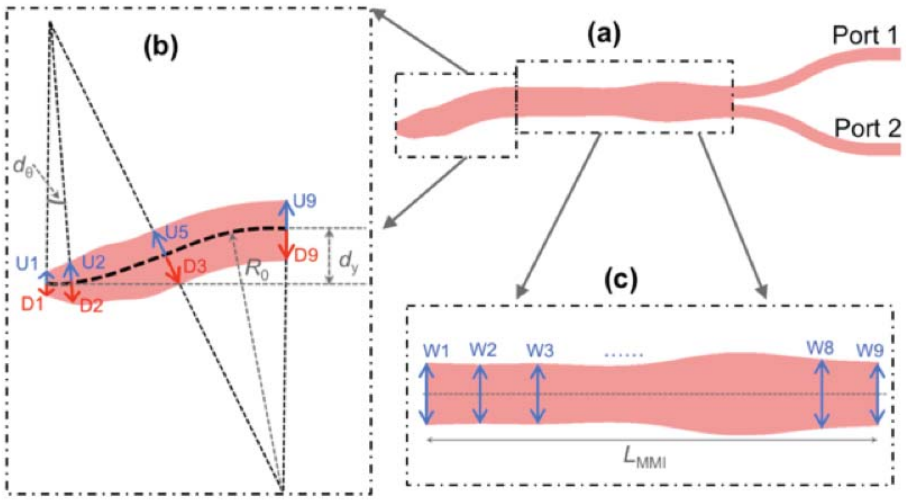

Figure 4-4 (a) Design of a diplexer consists of a bent taper cascaded with a PSO MMI. Light enters from the left end and splits at the right end into two S-bends with bend radius of 6 μm. (b). Detailed design parameters of a bent taper. (c). Detailed design parameters of the PSO MMI.

The overall schematic geometry of the diplexer design is shown in Figure 4-4(a). Light enters the left end to the bent taper, propagates in the PSO MMI region, and splits at the right end. The upper and lower ports are marked as Port 1 and Port 2 respectively. Note for both ports, a 0.8um long taper is used to connect the S-bend with the right end of PSO MMI. The input waveguide width at left end and the starting width of the tapers at the right are all 500 nm. In this paper, S-bend width of port1 is maintained 500nm and the width of port2 is tapered to 420nm to guide single mode 1310 nm signal. One can set other widths of interests for different target wavelengths.

Geometry detail of the proposed bent taper is shown in Figure 4-4 (b). The geometry engineering of the bent taper starts from a normal S-bend. Universally, an S-bend waveguide can be defined by three factors: center radius R_0, vertical offset *dy*, and waveguide width. In waveguide routing, it is common practice to avoid using multimode S-bend to eliminate multimode mixing. However, such multimode mixing can be of use if its behavior can be tailored. Instead of fixing the waveguide width as a constant, we choose to vary it at different angles. As seen in Figure 4-4 (b), we break the S-bend into 8 segments of equal angles, d_θ, and do interpolation between each segment to make the transitions smooth. The waveguide width of a S-bend is relative to the center radius R_0. The center radius R_0 divides the S-bend into the up side and the down side. We choose asymmetric widths to increase the optimization freedom. Therefore, we have two sets of independent width parameters: {*U1, U2, U3, ... , U9*} and {*D1, D2, D3, ... , D9*}, as indicated in Figure 4-4 (b).

The bent taper is then connected with the PSO MMI coupler, as depicted in Figure 4-4 (c). Similar to Ref. [34], the PSO MMI is symmetric and evenly divided into 8 parts by defining {*W1, W2, W3, ..., W9*}; interpolation is used to smooth the geometry. The simulations are carried out by Lumerical 3D FDTD Solutions. Material dispersion is a built-in property of the simulation tool.

Optimization is divided into two phases. First, we optimize the bent taper. In this phase we take the PSO MMI as a normal MMI with constant width, i.e., *W1 = W2 = W3 =.... = W9 = W*. Here *W* is chosen to be 1.25 μm so after connecting the MMI with two lead out waveguides, it still leaves a 250 nm gap in between S-bends to avoid violating the minimum feature size rule of a CMOS-compatible fabrication process. We also fix L_{MMI} to be 8 μm. Note that {*Wi*} and L_{MMI} may change in the second

optimization phase. The vertical offset, d_y, of the bent taper is set to be 1.1 μm. We then optimize the center radius R_0 as well as the S-bend width parameters $\{Ui\}$ and $\{Di\}$. Since the design goal is to reach a highly-efficient wavelength diplexer, the design figure of merit (FOM) in this step was chosen to be the average transmittance of the two-targeted wavelengths, i.e., FOM = $[T(\lambda_1) + T(\lambda_2)]/2$. Here we set λ_1 = 1550 nm, and λ_2 = 1310 nm. To make seamless connections, U1 and D1 at the narrow end are both fixed to be 0.25 μm to connect with the input single mode waveguide while U9 and D9 at the wide end are fixed to be 0.625 μm to connect with the MMI coupler. By only optimizing the R_0 and the first two segments (U2, U3 and D2, D3), a FOM = 88% can be reached. The rest of the parameters are kept the same for the wide end. Optimizing all the eight segments actually does not increase the FOM but forms sharp wavy geometries that are unwanted for fabrication. R_0 is found to be 6 μm after the first step of optimization. The length of the bent taper can thus be calculated to be 5.02 μm. The final width parameters $\{Ui\}$ and $\{Di\}$ of the bent taper are listed in Table 4-1. Note the nm resolution in Table 4-1 is rather the simulation accuracy than the required fabrication accuracy. Fabrication tolerance will be discussed later.

Table 4-1. Bent taper geometry parameters (μm)

U1	U2	U3	U4	U5	U6	U7	U8	U9
0.25	0.479	0.648	0.625	0.625	0.625	0.625	0.625	0.625
D1	D2	D3	D4	D5	D6	D7	D8	D9
0.25	0.472	0.49	0.625	0.625	0.625	0.625	0.625	0.625

Table 4-2. PSO MMI geometry parameters (μm)

W1	W2	W3	W4	W5	W6	W7	W8	W9
1.250	1.200	1.224	1.146	1.240	1.600	1.630	1.396	1.286

The second phase is to optimize the MMI part to further increase the diplexing efficiency and to balance the performance of each port. By taking the degree of unbalance of the two ports into consideration, we modify the FOM to be $[T(\lambda_1) + T(\lambda_2)]/2 - |T(\lambda_1) - T(\lambda_2)|$. In this step we optimize *W2* to *W9* as well as L_{MMI}. *W1* is fixed to be 1.25 μm to make the connection with the bent taper. With L_{MMI} = 9.173 μm and $\{Wi\}$ as listed in Table 4-2, the best FOM is found to be 95.3%. Note the slowly varying geometry of the final PSO MMI shown in Figure 4-4(c) is suitable for fabrication.

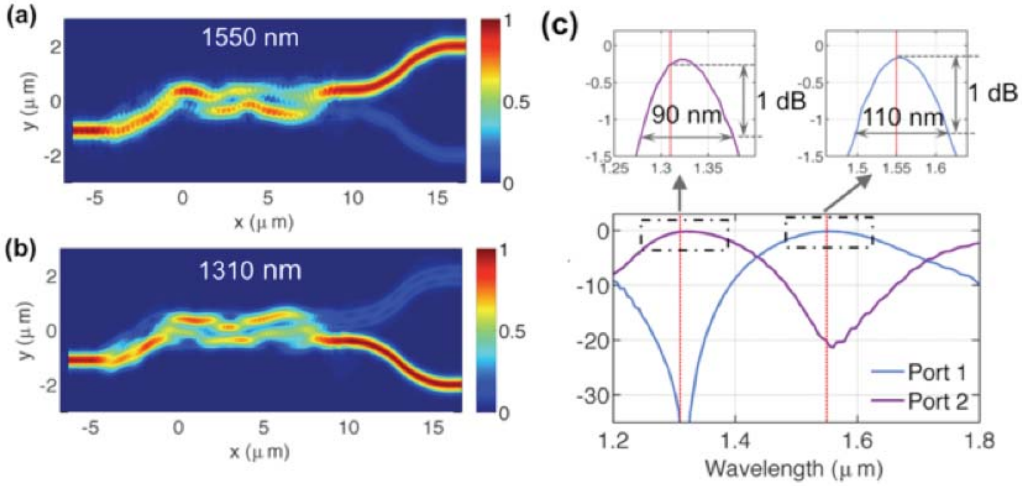

Figure 4-5. Simulated performance. (a) E-field at 1550 nm (b) E-field at 1310 nm. (c) Output spectrum of the two ports. The vertical red lines indicate 1310 nm and 1550 nm.

Table 4-3. Comparison to other integrated diplexer designs

Structure	Material	Wavelengths (nm)	Foot Print (μm^2)	Insertion Loss (dB) *[a]	Crosstalk (dB) *[a]	1-dB Bandwidth (nm)
Grating coupler [89]	SOI	1310/1490	10 × 10 *[b]	2.6	− 15	~ 25
Grating coupler [90]	SOI	1270/1577	11 × 11*[b]	5	− 20	N.A.
Ring resonator [91]	SOI	1534.4/1535.4	12 × 12	~ 1	− 15	< 0.2
MMI coupler [38]	SOI	1300/1550	980 × 6	0.23	− 22	~ 90
MMI coupler [93]	III-V	1310/1550	963 × 9	1.46	− 12	N.A.
MMI coupler [94]	SOI slot	1300/1550	119 × 3	0.2	− 26	N.A.
This work	SOI	1310/1550	15 × 2	0.25	− 20	90

*[a]. Showing weaker case of the two wavelengths.
*[b]. Foot print of the grating region only. The footprint of the adiabatic taper of a grating coupler is not reported in these publications.

E-field plots in Figure 4-5 (a) and (b) clearly show the diplexing functionality of the design. Both wavelengths enter from the left end. Within a footprint of less than 15 × 2 μm^2, 1550 nm is efficiently routed to port 1 and 1310 nm to port 2 with very weak crosstalk as well as scattering. The performance is plotted in Figure 4-5 (c). The peaks are closely centered around 1310 nm and 1550 nm, respectively, as indicated by the red lines. Crosstalk is below -20 dB at both ports. Note that for the most common use of a diplexer (in PONs) this crosstalk is not pertinent as the light for the two bands is traveling in opposite directions.

This design also offers a very wide bandwidth as seen from the two insets at the top of Figure 4-5 (c), which are magnified plots around the peak wavelengths. Port 1 has a 1dB bandwidth of 110 nm with a peak efficiency of 96.1 % (i.e., 0.17 dB insertion loss) and port 2 has a bandwidth of 90 nm with a peak efficiency of 94.4% (

i.e., 0.25 dB insertion loss). The numerical simulation results showed that a bent taper can be engineered to be a powerful mode-evolution device. Together with a PSO MMI, a very efficient wavelength diplexer is realized within an ultra-compact footprint. A comparison of the performance of our diplexer to other integrated diplexer designs is shown in Table 4-3 with the key metrics listed.

4.2.3 Yield analysis

Fabrication robustness is one of the key considerations for any devices aimed for real CMOS-compatible production. For MMI-type silicon photonics devices, the uncertainty of lateral dimension (width, W) and the vertical dimension (thickness, H) are two main factors.

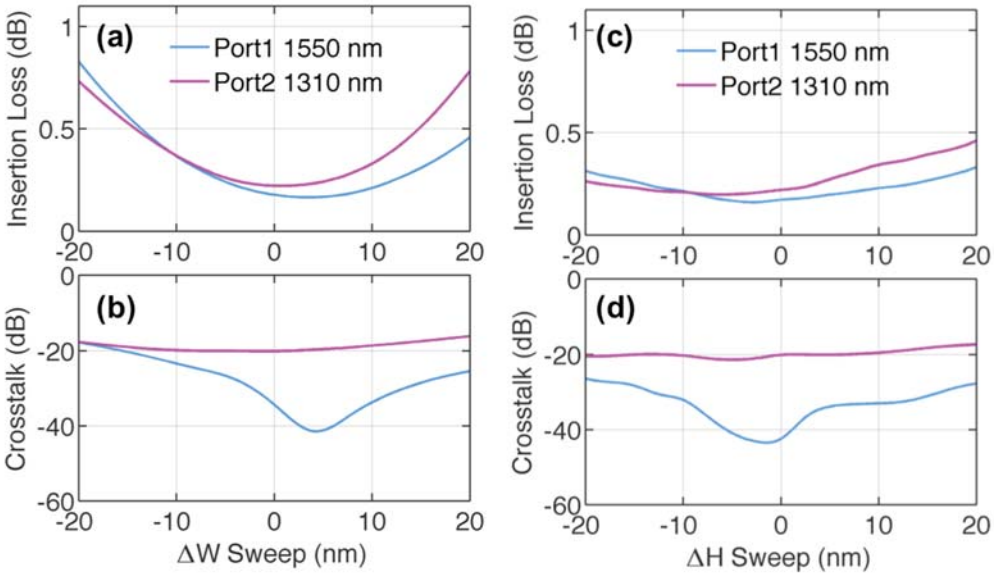

Figure 4-6. Yield analysis. (a) and (b). Sweep of width deviation. (c) and (d) Sweep of thickness deviation.

As discussed before, an MMI-coupler-based diplexer with smaller W_{MMI} is more vulnerable to fabrication uncertainty since L_π is more sensitive to the change of W_{MMI}. Such a device must have a compact footprint to maintain its robustness. We first performed yield analysis by sweeping the deviation of W_{MMI}, written as ΔW, to exam the fabrication tolerance of our design. It is worth noting that for the bent taper, ΔW needs to be distributed on both sides since it is asymmetric, i.e., $\{Ui + \Delta W/2\}$ and $\{Di + \Delta W/2\}$. But for PSO MMI, the width is defined by $\{Wi + \Delta W\}$. Although the real fabrication situation might be more complex, this analysis is a good approximation to examine the robustness of the design. The insertion loss and crosstalk at 1310 nm and 1550 nm are plotted in Figure 4-6 (a) and (b), respectively. Within a deviation of ± 20 nm in W_{MMI}, the insertion loss degradation is smaller than 0.6 dB for both wavelengths. The worst case for the crosstalk across the ± 20 nm deviation happens at ΔW = - 20 nm, but the value is still below - 15 dB for both wavelengths, as seen in Figure 4-6 (b).

We then swept the deviation of Si thickness, written as ΔH, since the thickness of SOI wafers is less well controlled than epitaxial grown III-V wafers. Within a range of 220 +/ - 20nm, both insertion loss and crosstalk are insensitive to the change of thickness, as shown in Figure 4-6 (c) and (d). The worst-case insertion loss is still smaller than 0.5 dB and crosstalk is below -18 dB. The yield analysis at both dimensions verifies that this design has high fabrication tolerance.

4.3 Ultra-Compact Polarization Rotator

4.3.1 State of on-chip polarization rotator in silicon

Polarization rotators are a family of rotators that are widely used in today's polarization-diversified circuits. In order to achieve polarization rotation, waveguide symmetry must be broken, either in the vertical dimension (air cladding, extra topping material) or in the lateral direction (multi-layer Si). Chen *et al.* [96] demonstrated a high-efficiency PR with a device length of 420 μm using an additional Si_3N_4 structure located on top of a silicon waveguide. Sacher *et al.* [97] presented an adiabatic bi-level taper polarization rotator-splitter (PSR) with a device length of 475 μm. Although CMOS-compatible PRs with a SiO_2 cladding can be achieved, the footprints of these devices are still very large. Surface plasmon polaritons (SPPs) based polarization rotators are proposed to have compact footprint but the insertion losses (IL) of these devices are considerably high (~ 2 dB). [98] Fabrication barriers must also be overcome to make SPP PRs fully compatible with the CMOS process. Therefore, for PRs, a legitimate question, is then: is it possible to realize CMOS-compatible PRs with small footprint and high conversion efficiency?

4.3.2 An ultra-compact PR design enabled by bent taper

In this section, I incorporate the bent taper idea into designing a high efficient, ultra-compact PR. As will be shown, 0.2dB insertion loss is realized within 15 μm device length. The design goal is to find the optimum geometric parameters of the proposed PR, which can achieve high polarization conversion efficiency (PCE) with the most compact footprints. To meet this goal, we choose the particle swarm optimization (PSO) method, which has been shown to be an effective technique in designing compact and high-performance passive devices [34,36].

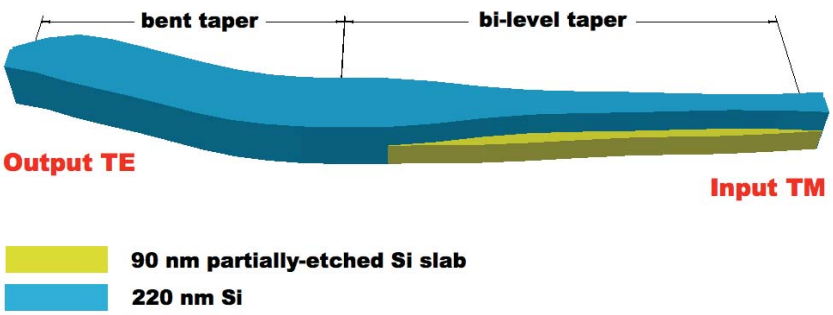

Figure 4-7. Schematic of the PR, consisting of a bi-layer taper and a bent taper. The PR is surrounded by a symmetric SiO_2 cladding (a buried oxide bottom-cladding and a SiO_2 top-cladding).

The basic idea is to use higher-order-mode-assisted mode rotation principle. Instead of rotating the mode directly, the higher-order-mode-assisted PRs use a higher order mode (usually a second-order mode, e.g. the TE1 or TM1 mode) as a transition between the two orthogonal modes (the TE0 and TM0 modes). Therefore the design can be separated into two parts, a TM0-TE1 rotator that is realized by a bi-layer taper and a TE1-TE0 rotator that is realized by bent taper. We can then combine these two parts to realize a TM0-TE0 PR, as sketched in Figure 4-7.

Linear adiabatic bi-layer tapers have been proven to be a good candidate for TM0-TE1 rotation with CMOS compatible fabrication processes [78,97]. By introducing a partial etched layer, waveguide symmetry is broken in the lateral dimension and mode hybridization can be realized. The mode conversion can be almost lossless in such a linear bi-level taper architecture. However, mode conversion is not efficient. The length of the linear adiabatic taper is usually around a hundred microns or even longer in order to achieve high conversion efficiency (> 95%).

Instead of using simple linear tapers, if one carefully engineers the taper geometry, one can expect improvement of the mode conversion efficiency.

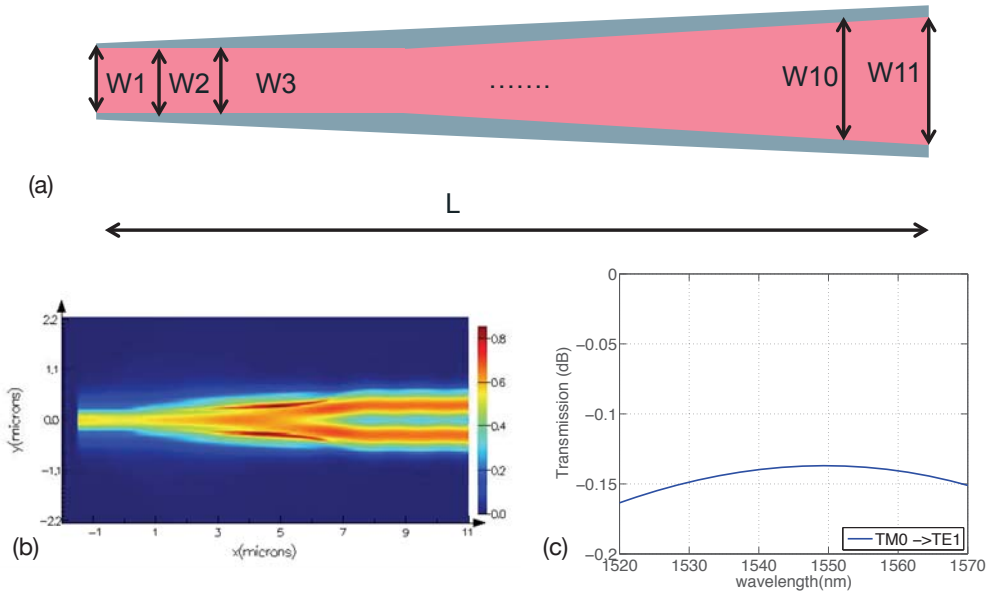

Figure 4-8. (a) Schematic of TM0-TE1 bi-layer taper. (b) E-field of the bi-layer taper convertor showing mode conversion from TM0 to TE1. (c) Simulated Loss.

Here, we use PSO method to design an ultra-efficient bi-layer mode converter. As shown in Figure 4-8 (a), the taper is symmetric and digitalized to 10 segments with interpolations between one another, similar to the PSO technique in designing the waveguide crossing [36]. Length of this bi-layer converter is fixed to only 9 μm during optimization, which is one order of magnitude smaller than any other previous demonstrations. The field pattern of this taper is shown in Figure 4-8 (b). TM0 mode is launched into the left side, and it quickly converts to a TE1 mode with minimum scattering loss. PCE higher than 96% (i.e., 0.17dB insertion loss as shown in Figure

4-8 (b)) is achieved across 50 nm wavelength ranges around 1550 nm. The widths of the ridge waveguide and partially-etched slab are listed in Table 4-4.

Table 4-4. Bi-layer taper geometry parameters (nm)

	W_1	W_2	W_3	W_4	W_5	W_6	W_7	W_8	W_9	W_{10}	W_{11}
Ridge	500	413	401	457	518	554	624	807	1077	1248	1250
Slab	500	648	759	795	848	960	1096	1191	1225	1237	1250

Different TE1-to-TE0 conversion schemes have been proposed in literature using different devices such as asymmetric directional coupler (DC) [85,99] and unbalanced MZI coupler [100,101]. However, each scheme has its own limitations. For example, the DC-based mode conversion scheme has an intrinsic bandwidth limitation, while the MZI-based mode conversion scheme is sensitive to fabrications as it depends on the exact phase-delay between arms.

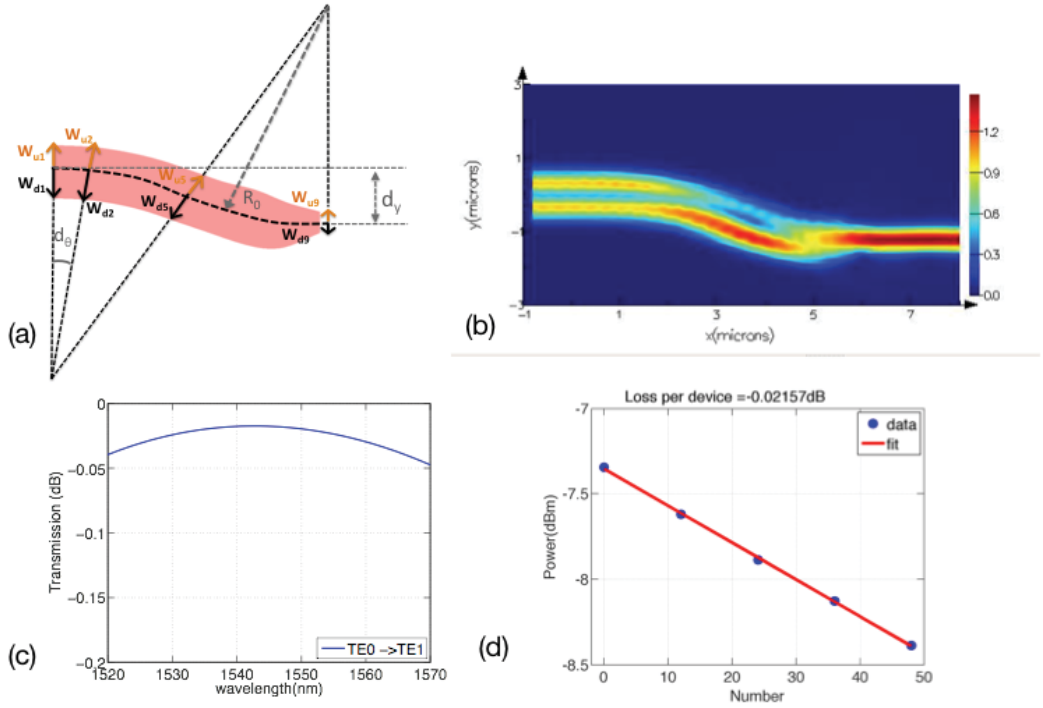

Figure 4-9. (a) Schematic of TE1-TE0 bent taper. (b) E-field of the tapering showing mode conversion from TE1 to TE0. (c) Simulated Loss as a function of wavelength. (d). Measured loss.

Here, I will demonstrate a wideband, compact and high-efficiency TE1-to-TE0 converter based on the bent taper idea that I proposed in section 4.1 . After optimizing the geometry with PSO, almost perfect mode conversion efficiency can be achieved within very short working distance. Schematic of the proposed design is shown in Figure 4-9 (a). Universally, a S-bend waveguide can be defined by three factors: center radius R_0, vertical offset d_y, and waveguide width W. W is a constant for a normal S-bend. Instead of fix the width W as a constant, we choose to vary W at different angles. We discrete the S-bend into 9 segments of equal angles, d_θ, and do interpolation between each segments to make the transition of geometry smooth.

Instead of defining symmetric S-bend (now relative to the center radius R_0) as in TM0-to-TE1 taper, we now choose asymmetric geometry for the S-bend to increase the optimization freedom. The center radius R_0 divides the S-bend into two sides: the up side and the down side. Therefore, we have two set of independent width parameters: $\{W_{u1}, W_{u2}, W_{u3}, \ldots, W_{u9}\}$ and $\{W_{d1}, W_{d2}, W_{d3}, \ldots, W_{d9}\}$, as indicated in Figure 4-9 (a).

The TE_1 mode is launched in at the wide end (left of Figure 4-9(a)), which has a waveguide width of 1.25 μm and the TE_0 mode emerges at the narrow end (right of Figure 4-9 (a)), which has a width of 0.5 μm. Note that the 1.25 μm wide end is so chosen to be consistent with the above optimized TM0-to-TE1 convertor while the 0.5 μm narrow end is the standard width of our single mode waveguide for waveguide routing.

Table 4-5. TE1-TE0 bent taper geometry parameters (nm)

Wu_1	Wu_2	Wu_3	Wu_4	Wu_5	Wu_6	Wu_7	Wu_8	Wu_9
625	625	625	625	625	625	616	426	250

Wd_1	Wd_2	Wd_3	Wd_4	Wd_5	Wd_6	Wd_7	Wd_8	Wd_9
625	625	625	625	625	625	695	635	250

During optimization, we fix the vertical offset d_y to be 1.2 μm, and optimize the center radius R_0 as well as the waveguide width. We found that lossless conversion (99.5% efficiency, Figure 4-9 (c)) can be achieved by only optimizing the center radius and the last two segments (W_{u7}, W_{u8} and W_{d7}, W_{d8}). The first 6 segments were kept the same as the wide end, which has a width of 1.25 μm. R_0 is found to be 8.531 μm after optimization. Length of the bend taper can thus be calculated to be 6.3 μm.

The detailed geometric parameters are provided in Table II. The measured device loss is given in Figure 4-9 (d), showing 0.02 dB loss, which matches with the simulation very well. Generally speaking, TE_1 mode can be effectively regarded as combination of two anti-phase TE0-ish modes. The phase mismatch must be overcome to convert TE1 into TE0 mode. As seen in Figure 4-9 (b), this ultra-compact bent taper design allows the two anti-phase components of TE_1 mode to travel with different effective lengths and eventually adiabatically combined to the TE_0 mode at the narrow end. Meanwhile, since the mode conversion happens within a single waveguide, broadband performance is automatically achieved.

With demonstration of the TM0-TE1 bi-layer taper and TE1-TE0 bent taper, combining these two parts readily forms a TM0-TE0 PR. Figure 4-11 (a) clearly demonstrates the rotation of E-field from TM0 to TE0. While at TE0 input, most of the light get scattered and eventually becomes loss, which is a desirable in a PR since it reduces the crosstalk from TE0 that can be coupled from a polarization splitter or elsewhere. The loss of PR is < 0.25 dB with across C-band with <0.1 dB wavelength dependence. After the mode conversion, the extinction ratio of the remaining TM0 is less than – 40 dB. The crosstalk from TE0 to TM0 is also less than – 40 dB and the extinction of TE0 is less than – 24 dB.

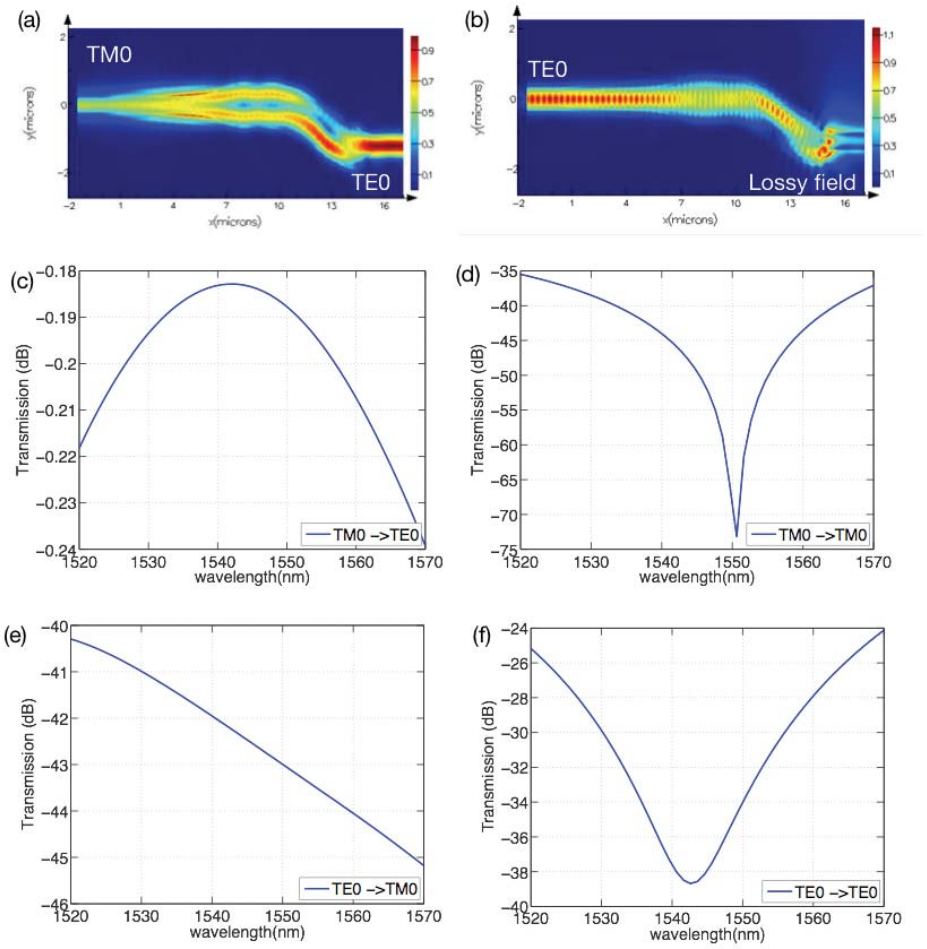

Figure 4-10. Performance of the PR. (a) E-field plot at TM0 input. (b) E-field plot at TE0 input (c) Insertion loss (TM0 to TE0) (d) Extinction ratio at TM0 mode (TM0 to TM0) (e) Crosstalk from TE0 to TM0 (f) Extinction ratio at TE0 mode (TE0 to TE0)

4.4 Symmetrical Polarization Splitter Rotator

4.4.1 Introduction

In addition to transistors, silicon-on-insulator (SOI) material has been proven to be a suitable substrate material for photonic devices, thanks to its high index contrast, tight manufacturing tolerances, compatibility with complementary metal-oxide semiconductor (CMOS) fabrication processes. [102] Building photonics in SOI also offers paths to integration with CMOS and bipolar electronics, either monolithically or through bonding-based integration. [49,103,104] One of the central challenges in developing practical silicon photonic systems-on-chip is to address the polarization incompatibility between a circular single mode fiber and a rectangular on-chip waveguide.

Polarization in an on-chip waveguide is restrained to transverse electrical (TE) and transverse magnetic (TM), which by default have very different effective indices, unless the waveguide is either low-confinement or square. In a single mode fiber, polarization is not maintained but instead changes randomly with environmental variations, causing random projections of TE and TM to an on-chip waveguide. This is a serious issue for many on-chip designs, especially receivers. [50] For low-cost, high-volume applications, being able to deal gracefully with both polarizations is of the essence. For anything inside the network – switches, ROADM's, attenuators – and for receivers, it has historically been the case that devices were constrained to accepting both polarizations. Historically, most optical devices for data transmission systems have been forced to be polarization-independent, with the exception of lasers (typically transmitting TE polarization) and sometimes modulators (often connected to the laser with expensive polarization maintaining fiber, and accepting only single-

polarization input). Considerable engineering went into developing devices with low polarization dependent loss (PDL). [105–107]

In silicon photonics, we have an opportunity to leverage complexity in order to deal with polarization – by creating a single polarization splitter/rotator (PSR) device which both splits and rotates the polarizations of the fiber into two parallel but physically separate channels on-chip, we can achieve low PDL without forcing the entire on-chip device library to deal with both polarizations. [60] Given the ability to very easily scale to complex systems-on-chip, this plays to the advantages of the silicon photonics platform. However, this approach depends on having low PDL, high performance PSR devices.

To address the issue, major silicon photonics platforms gravitate toward to two types of SOI thickness: multi-micron SOI (usually 3um) with low-confinement modes [39,40] and submicron SOI (usually 220nm, 250nm, or 300nm) [37,41–43]. For multi-micron SOI waveguides, polarization independent circuits can be built due to low confinement of optical modes. However, it requires very large bend radius (250 μm in [44]) to avoid excitation of higher order modes. This type of silicon photonics platforms become less promising when it comes to dense and energy efficient photonic integration using devices like micro-ring modulators [45,46]. It is also challenging to build efficient high-speed Mach-Zehnder modulators and photo detectors in such a platform.

Presently, submicron platforms are emerging as the dominant ones for large-scale integration. The width of a single mode waveguide in such platform is usually ~2 times larger than its thickness in order to provide strong mode confinement, thus enabling tight bends (radius <2.5 μm in [45]). But high polarization dependence

(birefringence) is introduced at the same time. The performance of photonic devices such as directional couplers and modulators is usually very different for TE and TM modes. For submicron platforms, polarization conversion is needed at the interface between optical fiber and on chip photonic integrated circuits (PIC). After light is coupled onto the silicon chip, a polarization splitter and rotator (PSR) is used to separate the incoming TE and TM light component and convert them into TE modes at the two output ports, so that the remainder of the PIC can operate in only one mode.

Many efforts have been made to improve performance of the PSRs on SOI platforms, especially in the past four years. In some cases, polarization splitter [108–110] and polarization rotator [96,111,112] are reported individually. One can construct a PSR by combining a splitter followed by a rotator. [85,97,101,113–115] While in other designs, polarization splitting and rotating happens simultaneously. [116–119] To characterize a PSR, important metrics such as polarization conversion efficiency (PCE), insertion loss (IL), polarization crosstalk, polarization dependent loss (PDL) as well as footprint, fabrication complexity, and fabrication tolerance must be considered. The state-of-the-art experimentally demonstrated performance of CMOS compatible PSRs have > 97% PCE, ~ 0.5-1 dB IL, 1 dB PDL and −15 dB crosstalk with device lengths vary from ~20 to ~ 500 μm. [97,114,117,120]

To the best of our knowledge, all reported PSR designs use pure TE0 and TM0 mode as basis set. That is to say, the incoming TE0 component is directed to one output port, while TM0 component is directed to the other port (rotated to TE0 mode). However, the separation of pure TE0 from the TM0 mode is not required. In fact, the State Of Polarization (SOP) of the input optical signal has been scrambled in the

optical fiber during transmission, and the pure TE0 and TM0 component does not hold a unique advantage over other orthogonal bases. By breaking this constraint, we have a much wider design space, which enables us to build more optimal devices.

In this part I introduce a novel PSR that utilizes the linear combination of TE0 and TM0 as orthogonal bases. The orthogonal bases of this PSR are rotated by 45 degrees compared with conventional PSRs, in other words, 45deg polarized incoming light relative to the orientation of the chip (TE0+/−TM0) is fully directed to one output. This design is symmetric in geometry, offers great design freedom to eliminate polarization dependent loss (PDL), and is easy to realize. This design also presents a new perspective for integrated PSR designs in the future. Then, I propose an optimized ultra-compact 45-degree PSR design with 12 μm device length, < 0.1 dB PDL, < 0.4dB simulated IL and < 0.05dB wavelength dependence across C-band for both polarizations.

4.4.2 Principle of the 45-degree PSR

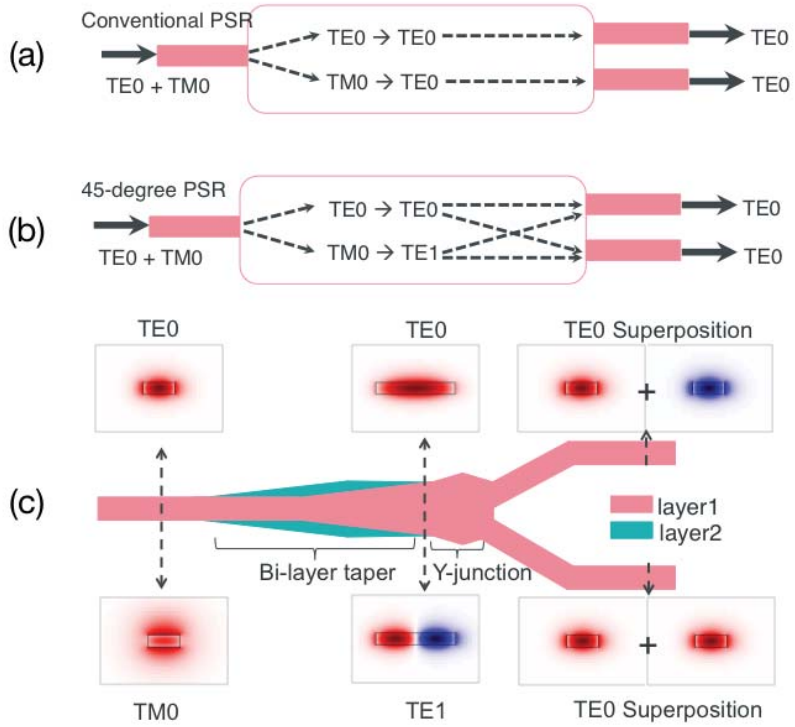

Figure 4-11. Operation principle of (a) a conventional PSR and (b) a 45-deg PSR. (c) Schematics of the 45-deg PSR and its mode evolutions.

A PSR is a device that converts the two orthogonally polarized modes received from the fiber into two copolarized, spatially separated modes. [121] Supposing TE0 goes to top branch and TM0 goes to bottom branch (rotated to TE0) at the output ports, the relation between output modes (E_{TE0}^{top} and E_{TE0}^{bot}) and input modes (E_{TE0}^{in} and E_{TM0}^{in}) could be expressed as

$$\begin{bmatrix} E_{TE0}^{top} \\ E_{TE0}^{bot} \end{bmatrix} = J \begin{bmatrix} E_{TE0}^{in} \\ E_{TM0}^{in} \end{bmatrix}, \tag{4-3}$$

where J is the Jones' matrix of PSR. From the definition, any device with unitary Jones' matrix can serve as a PSR.

Figure 4-11 (a) shows the principle of conventional PSR. The goal of a conventional PSR is to separate TE0 and TM0 and rotate TM0 into TE0. For ideal conditions (no IL and no polarization crosstalk), we write J for conventional PSR,

$$J = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \tag{4-4}$$

Figure 4-11 (b) shows the principle of a 45-degree PSR. As light propagates along the device, the TM0 mode is first rotated into a TE1 mode by a rotator while the TE0 mode is left undisturbed. The TE0 and TE1 modes are then separated in a splitter, which produces two distinct TE0 modes. The splitter functions as a 3dB divider and can be implemented with a symmetric Y-junction.

A detailed schematic of a 45-degree PSR showing the spatial evolution of the mode profile is illustrated in Figure 4-11 (c). The TM0-to-TE1 rotation is realized by a Si bi-layer taper similar to those referenced in [78,97]. Both TE1 and undisturbed TE0 mode are then split via a Y-junction. The Jones' matrix for an ideal 45-degree PSR is:

$$J = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix}. \tag{4-5}$$

For a pure TE0 input, the input vector is [1,0], the output is [1/√2, 1/√2] which means the optical field in the top and bottom output waveguides are equal and in phase. Similarly, for pure TM0 input [0,1], the output optical fields are equal but out of phase. If an input polarization is 45deg polarized [1, 1] or [1, −1], the output can be completely routed to the top or bottom output waveguide, respectively.

From the above explanation, it is clear that the orthogonal bases on the PSR have been rotated by 45 degrees compared with conventional designs.

4.4.3 A prototype PSR

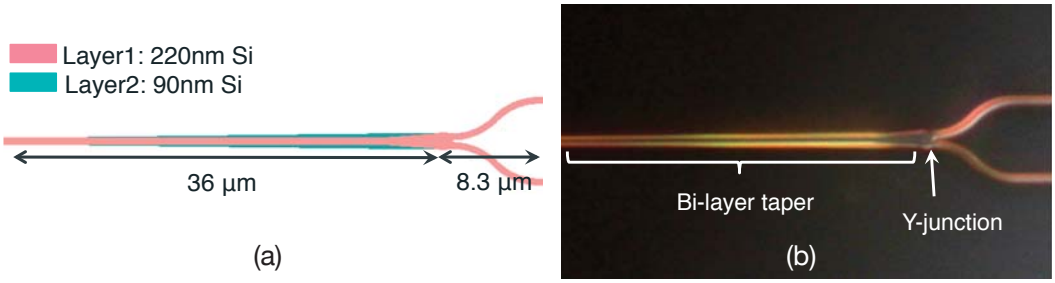

Figure 4-12. (a) Layout of the prototype 45-degree PSR design. (b). Micrograph of the fabricated device.

Based on the principles stated above, a prototype 45-degree PSR is designed from a linear bi-layer taper followed by a Y-junction on 220nm SOI, as shown in Figure 4-12 (a). The total device length is 44.3 µm, including the routing bends of the Y-junction. The simulated insertion loss is 0.68 dB for TE0 and 0.78 dB for TM0. The device fabricated using a 248nm lithography CMOS-compatible process on an 8-inch SOI wafer through an OpSIS-IME multi-project-wafer run [41]. A micrograph of the fabricated prototype PSR is given in Figure 4-12(b). To prove the concept of the PSR, we implemented it into a polarization insensitive receiver system, which will be discussed in detail in chapter 5.2 .

4.4.4 An improved ultra-compact 45-degree PSR

The prototype of the 45-degree PSR we designed has a simulated loss of 0.68 dB for TE0 and 0.78 dB for TM0 with ~50 μm device length. There is still much space left for improvement. Since the entire device is symmetric in geometry, it is well suited for finite difference time domain (FDTD) coupled particle swarm optimization (PSO), as we've demonstrated in designing high performance waveguide Y-junction and crossing [34,36]. The optimization can be divided into two stages. The first stage is to optimize the TM0-to-TE1 bi-layer taper. Here we migrate the same bi-layer taper (9 μm long, 97% PCE) in Table 4-4 as in our ultra-compact polarization rotator design [112]. Adiabatic linear tapers can be used if footprint is not a constraint. The second stage is to optimize a Y-junction, therefore procedures in [34] can be used.

Following this method, we realized an improved 45-degree PSR design. The design has very low and well-balanced insertion loss: ~ 0.35dB for TE0 and ~ 0.25 dB for TM0 (Figure 4-13 (a)), with PDL < 0.1dB across 1520nm–1570nm (more than entire C-band). It's worth noting that TM0 loss here is 0.1 dB lower than TE0, which is hard for conventional asymmetric PSRs since extra loss is often introduced when rotating TM0 to TE0. Moreover, the Y-junction part offers great design freedom to control PDL, regardless of the assistance of PSO. In some cases, it is even possible to design a PSR that has compensated PDL of edge coupler. Since no directional-coupler-like structure is introduced, the device is also ultra-broadband. For both polarizations, the wavelength dependence is < 0.05 dB across 50nm range.

The output transmittance as a function of polarization angle (consider linear polarization) is also simulated (Figure 4-13 (b)). The power equally splits at single TE0 (0 degree and 180 degree) and TM0 (90 degree) input. While at equalized TE0 and TM0 components (~45 degree and ~135 degree), the power is mainly routed to

only one branch (bottom branch and top branch for 45 degree and 135 degree, respectively). This is the major feature of 45-degree PSR. Note that in real designs, the angle may slightly shift from 45-degree due to PDL. The polarization crosstalk can be read at the null point of either branch, which is around –17 dB.

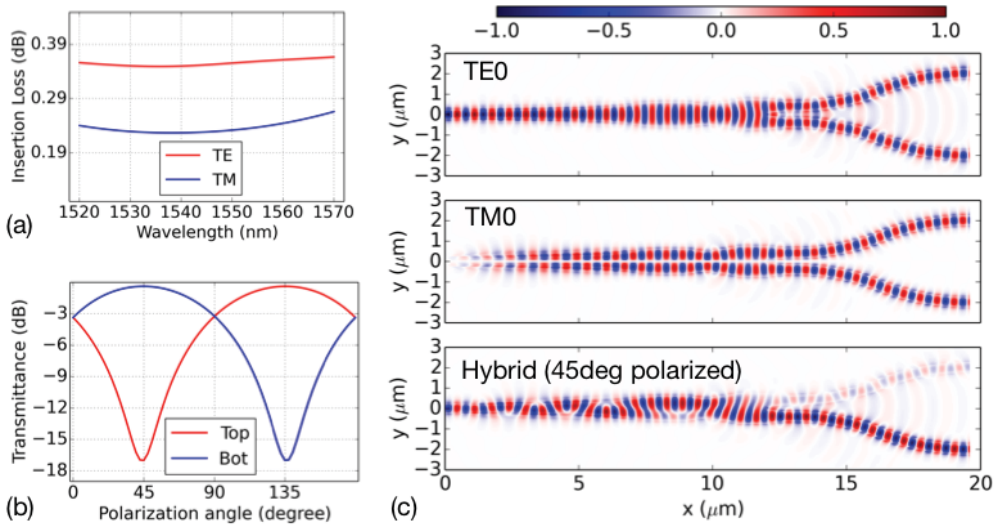

Figure 4-13. (a) Simulated insertion loss of TE and TM polarization. (b) Normalized output transmittance as a function of polarization angle for top and bottom branch. (c) E-filed distribution at TE0 input (top), TM0 input (middle) and hybrid polarization with equal combination of TE0 and TM0 (bottom).

Figure 4-13 (c) demonstrates how the 45-degree PSR functions with E-field plot at three specific input polarizations sates: TE0 (top), TM0 (middle) and 45-degree polarization (bottom). One can clearly see the in-phase output for TE0, anti-phase output for TM0 and single branch output (with weak crosstalk) at 45-degree polarization. The device is ultra-compact, only 12 μm excluding the routing waveguide bends (20 μm if these are included).

We compared our proposed design with reported state-of-the-art PSRs in silicon. With comparable insertion loss of TE0 mode, our design is outstanding in terms of device length and PDL, as plotted in Figure 4-14.

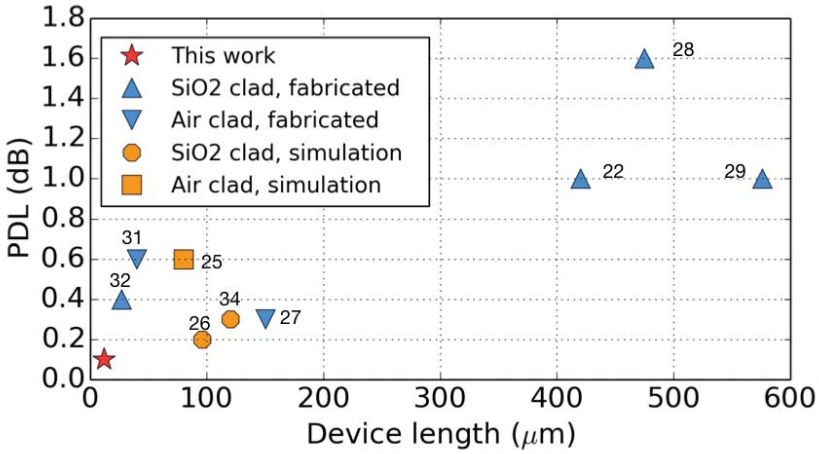

Figure 4-14. Comparison of our proposed symmetrical PSR design with previously reported PSRs based on SOI platform (PDL and device length). The numbers next to the markers indicate the references.

Chapter 5

ACTIVE COMPONENTS AND SYSTEM LEVEL INTEGRATION

5.1 High Speed Ring Modulators At 1310nm

5.1.1 Introduction

The 1310 nm wavelength band is of particular interest to data communications, owe to its capability of working beyond the dispersion limit at high bit-rate over considerably long distance. One of the critical components in this data communication is the modulator design. Very recently, National University of Singapore reported a 50 Gb/s traveling wave Mach- Zehnder (TWMZ) modulator near 1300 nm [9].

Ring-resonator-based devices have become a powerful tool for a variety of applications in silicon photonics links, such as signal modulation, switching and filtering. Much progress has been made in the past 10 years in silicon ring resonator modulators [7,122–124]. Compared to TWMZ modulators, ring resonator based silicon modulators produce much better performance in low power consumption, high modulation efficiency, small footprint and high speed due its small capacitance and compact size. However, to the best of our knowledge, all the ring resonator modulators that have been reported are working near 1550 nm band.

In this work, we report a high-speed silicon microring modulator near 1310 nm with 3dB bandwidth of 28 – 40 GHz, depending on its operation wavelength. A highly efficient (253 pm/mW) ring filter near 1310 nm is also presented here to serve as tunable filter for wavelength division multiplexing (WDM) designs. This is the first

high-speed silicon micro-ring modulator demonstrated near 1310nm to the best of our knowledge. Lastly, we perform 40 Gbps NRZ-OOK data transmission through 40 km with standard single mode fiber. The energy efficiency is 115 fJ/bit. Our work shows that the data link suffers negligible dispersion penalty. This makes the modulator a potential candidate for high-density, DSP-free metro network applications.

5.1.2 Design and fabrication

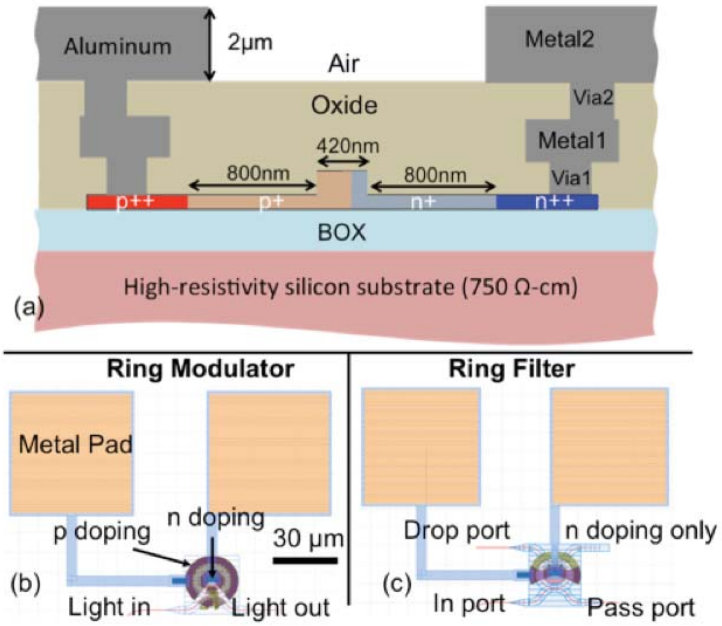

Figure 5-1. (a) Schematic cross sectional diagram of ring modulator, not to scale. (b) Layout of ring modulator. (c) Layout of ring filter.

5.1.3 Ring Modulator Characterization

Figure 5-1 (a) illustrates the cross-section of the pn junction design with key dimensions noted. The device fabrication was at the Institute of Microelectronics (IME), A*STAR, Singapore, through an OpSIS-multi-project-wafer run. The fabrication process was similar to that of [9]. The junction formed on striploaded ridge waveguide with a slab thickness of 90 nm and ridge height of 220nm. The width of the ridge is 420nm. The pn junction is slightly shifted from the center of waveguide for 50 nm to achieve higher efficiency. Figure 5-1 (b) shows the schematic of the ring modulator design with n-doping at the center, surround by p-doping. Figure 5-1 (c), ring filter is designed to only have n doping to form a thermal tuning resistor.

To achieve high modulation bandwidth and efficiency, quality (Q-) factor and extinction ratio (ER) are two check-and-balance parameters. High photon lifetime-limited bandwidth requires low Q-factor at the cost of reducing modulation efficiency. In our design, we use a symmetric directional coupler to couple light in/out of ring resonators with 2 μm coupling length and 0.25 μm coupling separation. As shown in Figure 5-2 (a), the Q-factor was measured to ~ 3400 while the ER remains > 30 dB. The photon lifetime-limited bandwidth is thus as high as 67 GHz.

The ring modulator's resonance shift was investigated by tuning DC bias voltages from 0.2V to -5V. The pn-junction tenability is 18 pm/V at small bias voltage, as seen in Figure 5-2 (b). The radius of ring resonator is 6.83 μm, resulting a free spectrum range (FSR) of 10.7 nm. The insertion loss of the device after doping is ~ 1dB, characterized by measuring a reference grating coupling pair spectrum nearby, as seen in inset of Figure 5-2 (b).

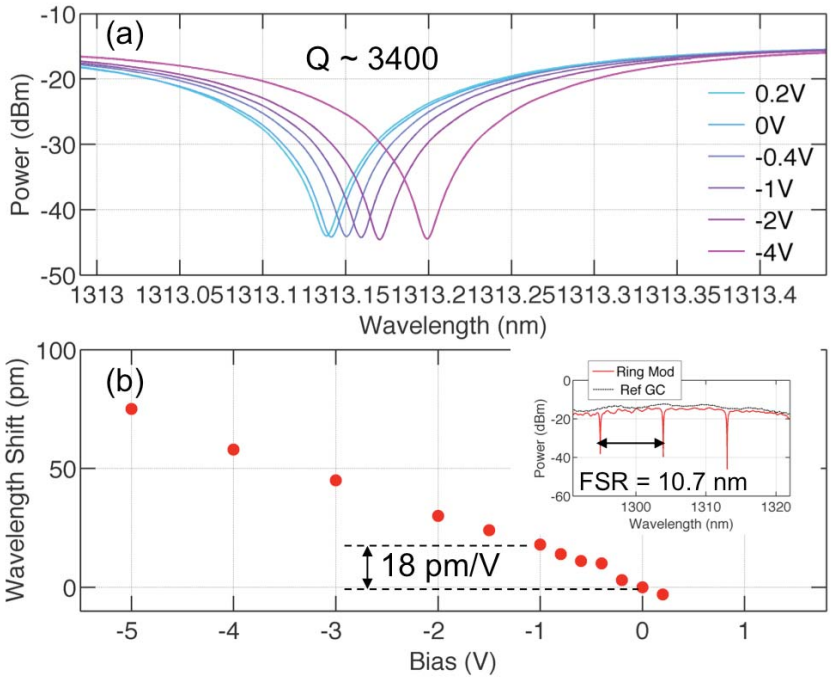

Figure 5-2. pn-junction tunability measurement of ring modulator. Inset shows the FSR and insertion loss with respect to a reference grating coupler.

The electro-optical (EO) modulation bandwidth was characterized by S-parameter measurement, calibrated from 100MHz to 50 GHz (Figure 5-3). Since photons with wavelength closer to the resonance will be trapped in the ring resonator longer, the EO bandwidth of microring is highly dependent on the operation bandwidth. [7,124] A single EO bandwidth without reporting which operation wavelength is of no important value in estimating data transmission speed. The operation wavelength can be defined in terms of power drop-off with respect the off-resonance power. For example, 3dB wavelength means the power at this operation wavelength is 3dB smaller than the off-resonance power.

Here we present in Figure 5-3 the measured EO S21 at -1V DC bias. The 3dB bandwidth was measured to be 40 GHz when operating at 3dB wavelength and 28 GHz at 6dB wavelength. The device is estimated to be workable at 40 Gbps and higher.

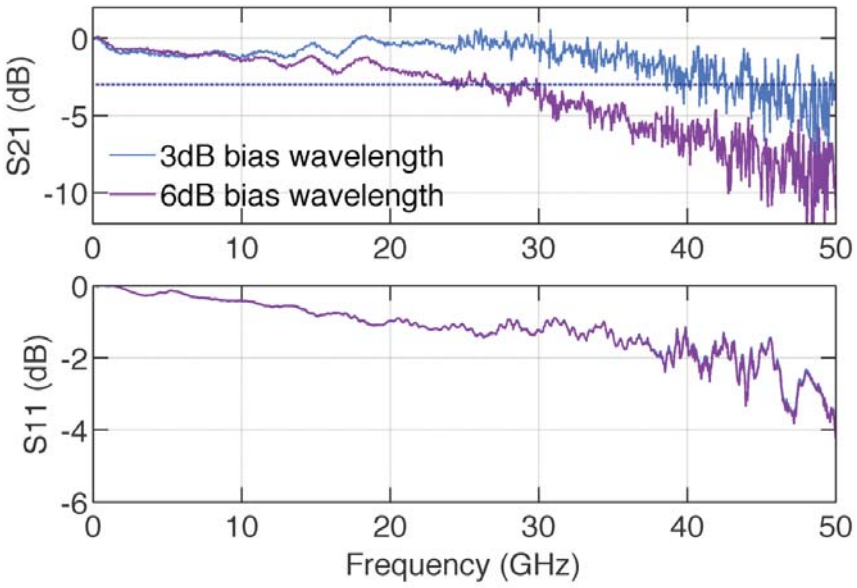

Figure 5-3. EO S-parameter measurement.

5.1.4 Ring Filter Characterization

The ring resonator can act as filter when the drop port is utilized to pick out the demanded signal at a certain wavelength. We use similar ring resonator structures as ring modulator but with only n+ doping to form a high efficient thermal tuner. Spectra of drop port were shown in Figure 5-4 (a) when tuned from 0V to 5V. The fitted thermal tenability is 253 pm/mW in Figure 5-4 (b). Only 36 mW is needed to tune a full FSR of 9 nm. As in inset of Figure 5-4 (b), after normalized with grating coupler

spectrum, the whole device has ~ 1 dB insertion loss and the drop port shows almost no extra loss at resonance. Q-factor of the pass port is ~ 1300.

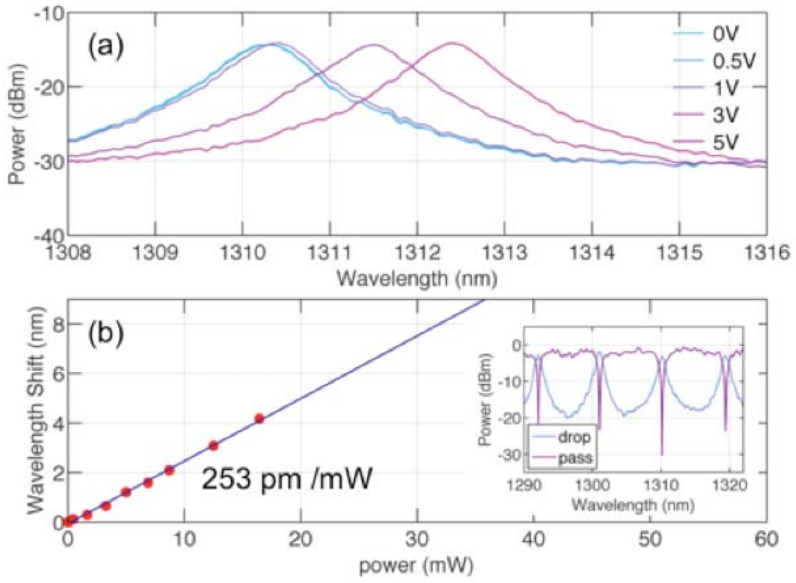

Figure 5-4. Thermal tunability measurement of ring filter. (a). Spectrum shift at different bias conditions. (b). Thermal tunability of ring filter. Inset shows FSR and filter spectra of drop port and pass port.

5.1.5 High speed dispersion-less data link

To demonstrate the dispersion-less link using the microring modulator and filter discussed above, 40Gbps NRZ-OOK signal, are transmitted through 40km standard single mode fiber (SSMF). The zero-dispersion wavelength (λ_0) of the fiber is first estimated using the setup in Figure 5-5 (a).

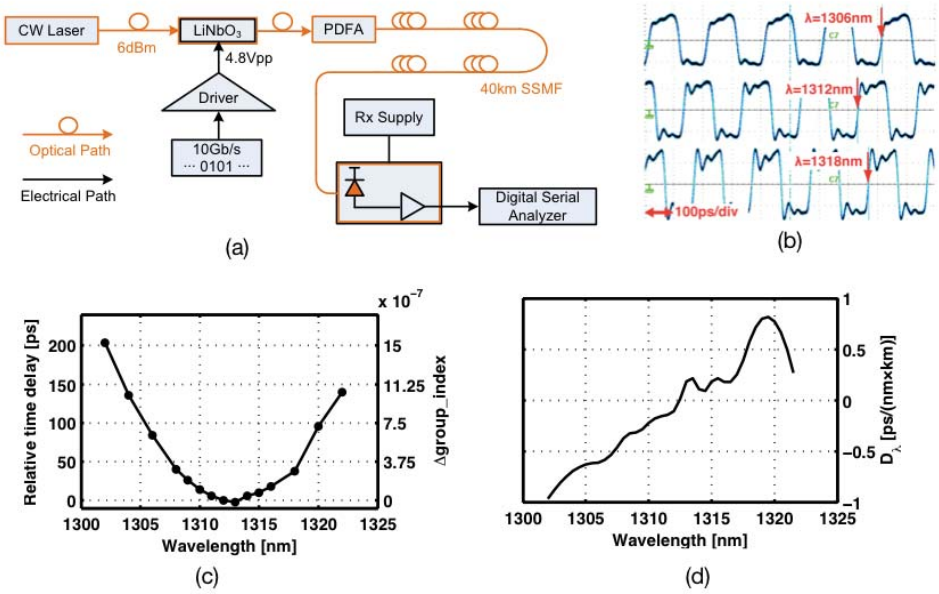

Figure 5-5. (a) Setup to track the pulse time delay through the 40km SSMF fiber. PDFA: praseodymium-doped fiber amplifier. $LiNbO_3$: commercial $LiNbO_3$-based Mach-Zehnder modulator. Rx: receiver. (b) The measured waveform as seen on oscilloscope at different wavelengths. The red arrows indicate the time stamp of the rising edge. (c) Measured relative time delay versus the wavelength. (d) Calculated chromatic dispersion curve.

The output of CW laser is modulated by the 10Gbps 0101 repeated pulse. By varying the laser wavelength, the pulse pattern would shift back and forth on the oscilloscope due to the different group velocity, which is illustrated in Figure 5-5 (b). The relation between relative time delay and the wavelength is established by tracking the time stamp of the rise edge. Since the time delay is proportional to the group index (N_g), the relative time delay can be directly converted to be ΔN_g, which is annotated on the right Y-axis of Figure 5-5 (c). By spline interpolating the data, the dispersion

curve can be approximated as $D_\lambda = \frac{\Delta N_g}{\Delta \lambda}$, as shown in Figure 5-5 (d). The estimated λ_0 is 1312.5nm.

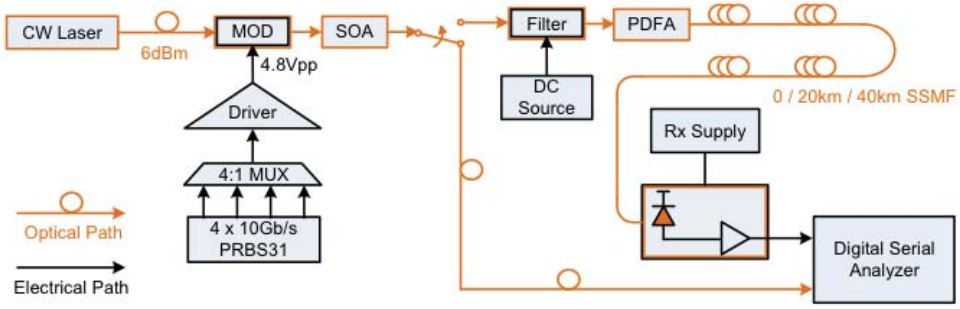

Figure 5-6. High-speed data link testbench. MOD: modulator. SOA: semiconductor optical amplifier.

The data link testbench is sketched in Figure 5-6. The 40Gb/s signal is generated from 4 x 10Gb/s NRZ PRBS31 stream, and amplified to $4.8V_{pp}$. The signal is then offset via a bias-tee and delivered to the modulator through a special GS probe. The probe has 50Ω shunt resistor at the tips to suppress the electrical back-reflection, which could have destroyed the amplifier. The tunable CW laser launches 6dBm power at into the modulator, the output of which is amplified by the SOA. The bias voltage and laser wavelength are tweaked against the optical eye of the SOA's output before feeding it into the filter. The final optical eye is shown in Figure 5-7 (a). The filter is thermally tuned to the laser's wavelength on its drop port by measuring the optical power. A PDFA boosts the drop's output to 12.5dBm, and launch it into the fiber. A commercial receiver picks up the signal at the end of spool and feed it into the oscilloscope. The resulted electrical eye is shown in Figure 5-7 (b)-(d). 1.2ps and

2.8ps jitter penalty through 20km and 40km fiber spool is observed as benchmarked by the eye taken immediate at the PDFA's output (0km).

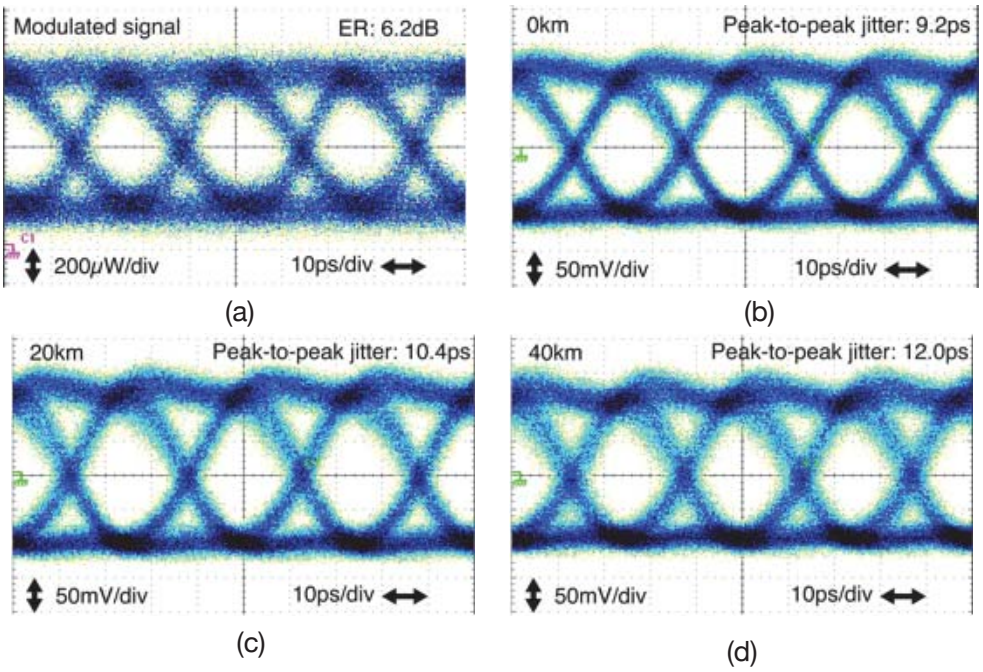

Figure 5-7. (a) Optical eye of the modulated signal. Junction bias: -2.6V. (b)-(d). Electrical eye after 0km/20km/40km transmission. The average power into the receiver is kept at -3.8dBm by adjusting the PDFA. CW laser wavelength: 1314.852nm.

Such a small jitter penalty is unsurprising since the laser is operated at 1314.852nm, 2.3nm away from λ_0. By approximating the signal bandwidth to 28GHz or 0.16nm, to the first order of approximation, the maximum dispersion can be estimated as 0.16nm × 40km × D_λ(1315nm) = 1.3ps, where D_λ=0.2ps/(nm×km) is read off Figure 5-5 (d). It's worth noting that 9.2nm FSR of the modulator implies an always-existing operating point no more than 4.6nm from the λ_0, regardless of the

specific SSMF used. The total link budget is 52, which includes ~24dB loss from 4 grating couplers, 16dB fiber loss, and 7dB modulator bias loss. The aforementioned poor tunability counts to the operation at such a lossy point to achieve the desirable extinction ratio. The link budget can be reduced by 12dB (2 couplers) with monolithic integrated modulators and filters, and further to 2dB with edge couplers [125].

Such small jitter degradation can be explained as follows: The laser is operated at 1314.852 nm, 2.3 nm away from λ_0. By approximating the signal spectrum width to 80 GHz (0.46 nm), to the first order of approximation, the CD through 40 km SSMF can be estimated as 0.46 nm × 40 km × D_λ = 3.7ps, where D_λ (λ = 1315nm) = 0.2 ps / (nm × km) is read from Figure 5-5 (d). In a general case, since the FSR is 9.2 nm, one can always find an operating wavelength no more than 4.6 nm (FSR/2) from λ_0, independent of the specific SSMF used. That implies an upper CD limit of 0.46 nm × 40 km × 4.6 nm × S_{0max} = 7.8 ps, where S_{0max} = 0.092 ps/(nm^2 × km) for ITU-T G.652 complaint fibers [126]. The 7.8 ps CD is tolerable for 40 Gb/s bit-stream. In addition, the thermal tuner can be employed to shift the resonance frequencies towards λ_0 at an efficiency of 0.2 nm/mW. Applying the proper tuning power and operating at λ can further reduce the CD_0.

One remaining question is the total link budget. While the link presented above has ~52 dB total loss (including 24 dB from four grating couplers) and utilizes two-stage optical amplification, it can be reduced to 27 dB by using low-loss edge coupler [127] (2 dB from two edge couplers, 2 dB on-chip loss, 7 dB bias loss of the modulator, and 16 dB from 40 km fiber). It can well fit into links with 6dBm laser input, −10 dBm receiver sensitivity and a moderate optical amplification (>11dB).

5.2 A Polarization Insensitive WDM Receiver System

As been discussed in chapter 4.4 , I proposed a novel PSR architecture. In order to prove the concept, I demonstrate here a four-channel polarization insensitive wavelength division multiplexing (PI-WDM) receiver (RX) employing a prototype 45-degree PSR. 40 Gb/s data rate with 0.7 +/− 0.2 dB PDL is achieved on each channel (highest single-channel data rate and lowest PDL among reported SOI PI-WDM RXs to date, to the best of our knowledge).

5.2.1 Design of a four-channel PI-WDM receiver

We constructed a four-channel polarization-insensitive wavelength division multiplexed (PI-WDM) receiver (RX) system. The schematic of the system is depicted in Figure 5-8 (a). Light with arbitrary polarization is first coupled to a Si nano-taper edge coupler from a lensed fiber and then separated by a 45-degree PSR, followed by two mirrored 1×4 WDM demultiplexers (DeMUXs). Schematic of the DeMUX is shown at the bottom of Figure 5-8 (a). Finally, the light in both branches combines at the gain peaking photo-detector (GPD) [17]. The four-channel WDM DeMUX consists of two stages of unbalanced MZI, as shown at bottom of Figure 5-8 (a). The MZIs have integrated thermal tuners to align the spectra. Performance of the thermal tuner is similar to our previous report. [128]

The entire receiver system has a footprint of 2.4 × 2.4 mm^2. A micrograph of fabricated system is shown in Figure 5-8 (b).

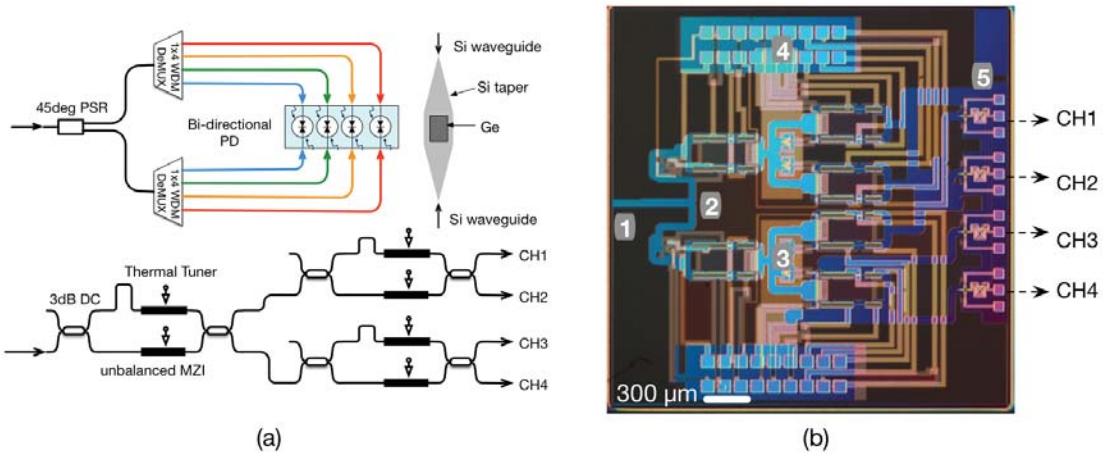

Figure 5-8. (a) Schematic of a four-channel PI-WDM receiver with illustration of a bi-directional PD (at right) and a 1×4 WDM DeMUX (at bottom). (b) Micrograph of the fabricated RX system. The key components are noted in numbers. #1: Si edge coupler; #2: 45-degree PSR; #3: 1×4 WDM DeMUX; #4: DC pads; #5: bi-directional PD.

5.2.2 PDL measurement

To characterize the RX system, the center wavelengths of the WDM DeMUX need to be aligned for all four channels. The four channels (CH1, CH2, CH3 and CH4) are defined in Figure 5-8 (a), corresponding to the four GPDs in micrograph of Figure 5-8 (b), counting from top to bottom, respectively. A rough spectrum alignment can be quickly achieved by sending CW laser input with scrambled polarization and correct wavelength while maximizing the photocurrent of each channel.

Rough aligned spectra are shown in Figure 5-9 (a). The channel spacing is measured to be 6.5nm. The entire spectra are well aligned across a 50nm range around 1550nm. Channel crosstalk is less than −11 dB. Figure 5-9 (b) depicts theoretical wavelength response of the WDM DeMUX for reference. Compared with theoretical calculations, channel crosstalk is degraded in the real system, due to alignment

accuracy as well as the non-ideal 3dB splitting ratio and wavelength dependence of the directional couplers (DCs).

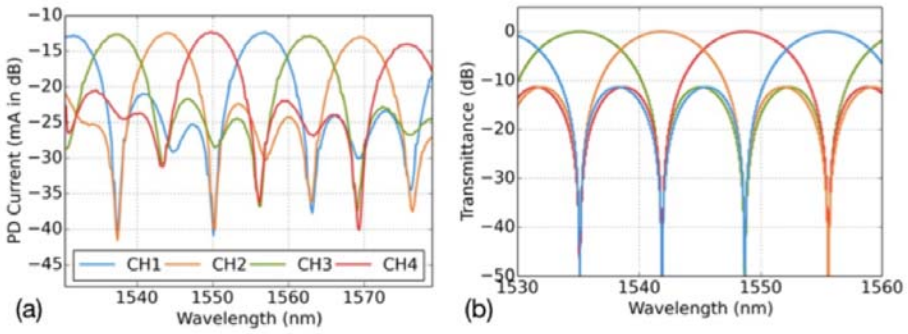

Figure 5-9. (a) Experimental rough aligned spectra with scrambled polarization. (b) Plot of DeMUX spectra based on transfer matrix model.

In order to measure the PDL in each channel accurately, we set up a 10 Gb/s non-return-to-zero on-off-keying (NRZ-OOK) data transmission link in combination with an inline wavelength sweep. The data link setup is sketched in Figure 5-10 (a). The tunable CW laser is first modulated by a commercial modulator with a 10 Gb/s PRBS2^{31}-1 (Pseudorandom binary sequence) data pattern and then amplified by an erbium-doped fiber amplifier (EDFA) to overcome the optical loss in the link. The amplified signal then goes through a polarization controller (PC) and a polarization scrambler (PS) before it is coupled to the RX chip. The GPD is biased at 2V through a bias-tee during measurement.

On each channel, we first enable the PS, fine tune the phase tuners in the DeMUX so the noise on the '0' and '1' rails on the eye diagram are minimized (recorded as 'On' condition). Then we disable the PS, and adjust the polarization

controller manually to find the polarization states where the eye amplitude is maximized (‘Off Max’ condition) or minimized (‘Off Min’ condition), and record the spectral sweep.

The eye diagrams are recorded in Figure 5-10 (b), showing good channel-to-channel uniformity. The inline spectrum sweeps are plotted in Figure 5-10 (c). The shaded area between Off Max and Off Min indicates PDL of each channel. As anticipated, scrambled (i.e., On condition) spectrum mostly sits inside the shaded area of related channel. Note the noise level is increased and shows strong wavelength dependence due to the introduction of an EDFA. The channels crosstalk is reduced from − 9 dB at 1530.5 nm (CH1) to – 14 dB at 1550 nm (CH4).

PDL is quantified from both eye amplitude and the spectrum sweeps, shown in Table 5-1. The PDL of eye diagram is calculated by dividing the amplitudes of Off Max and Off Min, i.e., $10\times log_{10}(Off\_Max/Off\_Min)$. The result is in the second row of Table 5-1. The PDL from sweeps can be simply calculated by subtracting photocurrents in dB scale. Row3–5 shows PDL regarding different wavelength ranges with respect to channel center wavelengths, to give a fair comparison. For clarity: Row 2 (“Eye Diagram”) represents the results of the eye-diagram based measurements of PDL, while rows 3-5 show the results of various ways of interpreting the swept spectrum measurements in order to extract the PDL. The two measurements align to within 0.35dB.

But overall, the results from sweeps match quite well with the eye diagram testing. CH1 and CH2 have slightly higher PDL from both eye diagram and wavelength sweeps, possibly due to slightly misalignment of the WDM DeMUX. Overall, the receiver demonstrates an excellent PDL of 0.7+/-0.2dB. This is higher

than the 0.1dB PDL predicted by the simulation on the 45-deg PSR. The extra PDL is introduced by the edge coupler, non-ideal 3dB DCs and unbalanced thermal tuner losses.

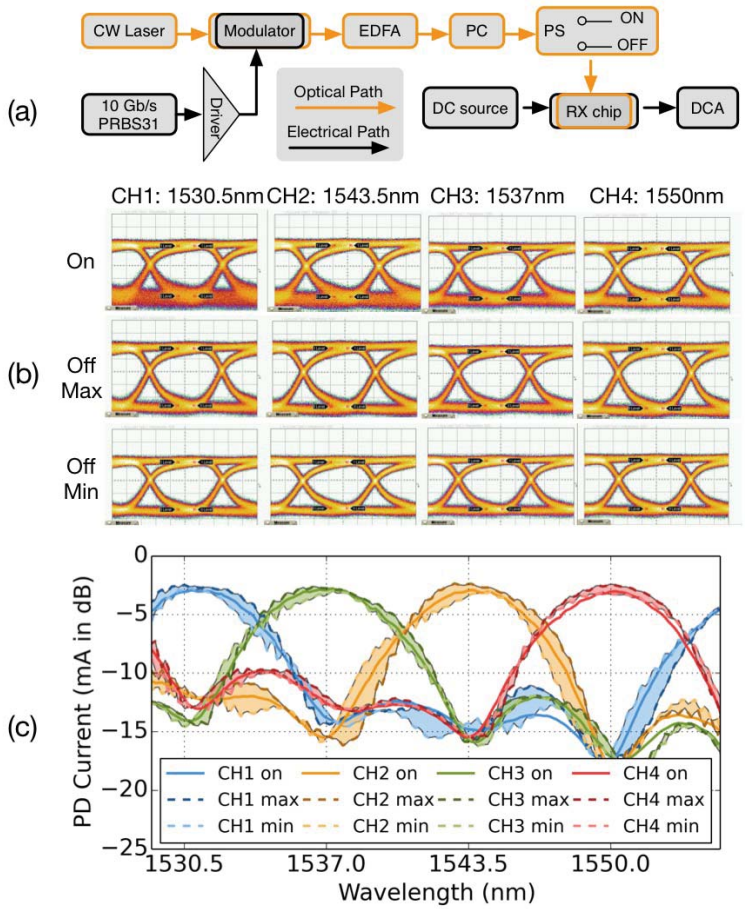

Figure 5-10. (a) High speed data link test bench. EDFA: Erbium-doped fiber amplifier; PC: polarization controller; PS: polarization scrambler; DCA: digital communication analyzer. (b). 10 Gb/s eye diagram of the RX (10mV/div vertically, 20ps/div horizontally). On: PS on; Off Max: PS off, maximum eye amplitude by tuning PC; Off Min: PS off, minimum eye amplitude by tuning PC. (c). Real-time spectrum sweeps with respect to the eye diagrams in (b).

During measurement, the input power to the chip is kept at 5dBm. Considering a typical 0.75 A/W responsivity at 2V bias [17], the received peak power can be calculate from Figure 5-10 (c) to be around −1.2 dBm. Thus, the total passive loss of the RX is about 6.2dB, including silicon edge coupler, 45-degree PSR, DeMUX, and the routing waveguides.

Table 5-1. Quantified PDL measurement

PDL (dB)	CH1	CH2	CH3	CH4	Avg	Std
Eye diagram	0.78	1	0.54	0.77	0.77	0.19
Peak wavelength	0.45	1.02	0.64	0.825	0.73	0.24
+/– 0.5 nm	0.48	0.99	0.53	0.71	0.68	0.23
Entire spectrum	0.74	1.08	0.52	0.52	0.72	0.26

5.2.3 40 Gb/s NRZ-OOK data transmission

The above PDL measurement in a 10 Gb/s data link has proven the functionality of the 45-degree PSR. Meanwhile, a PI-WDM system itself is interesting for investigation considering its importance in non-coherent silicon photonic detectors. [129–131] Therefore we further push our system from 10 Gb/s to 40 Gb/s. The data link setup is identical to that described previously, except for now we are using a 40Gb/s pulse pattern generator (PPG) with PRBS2^{31}-1 data pattern. The RF probe is switched to a 50-Ohm terminated configuration in order to reduce RF reflection as in [10,45] while bias voltage is changed from 2V to 4V to increase PD bandwidth.

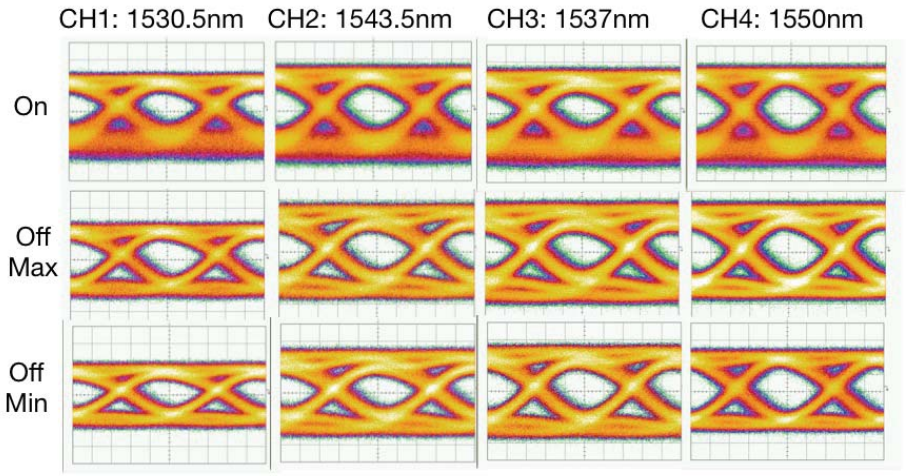

Figure 5-11. 40 Gb/s eye diagrams (3 mV/div vertically; 5 ps/div horizontally).

The measured 40Gb/s eye diagrams are shown in Figure 5-11. All four channels show open eyes with very good channel-to-channel uniformity. Also all the four channels present very small polarization dependence. PDL is estimated to be 0.3 – 0.8 dB by reading the amplitudes. Although the PDL estimation is less accurate than in the 10 Gb/s measurement due to larger noises in 40 Gb/s eye diagrams, the overall result is consistent. To conclude, we demonstrate 40Gb/s/channel data transmission in a PI-WDM RX system enabled by a novel 45-degree PSR. To the best of our knowledge, we believe this system reveals highest single-channel data rate with lowest PDL among reported PI-WDM RX on-chip systems to date.

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Appendix A

PUBLICATION LIST

1. Yangjin Ma, Yi Zhang, Shuyu Yang, Ari Novack, Ran Ding, Andy Eu-Jin Lim, Guo-Qiang Lo, Tom Baehr-Jones, and Michael Hochberg. "Ultralow loss single layer submicron silicon waveguide crossing for SOI optical interconnect." Optics express 21, no. 24 (2013): 29374-29382.
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Appendix B

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