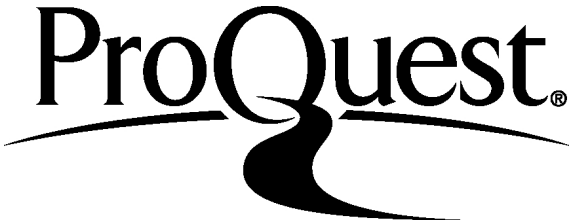
DESIGN AND CHARACTERIZATION OF A MIXED-SIGNAL PCB FOR DIGITAL-TO-ANALOG CONVERSION IN A MODULAR AND SCALABLE INFRARED SCENE PROJECTOR

by

Jacob Benedict

A thesis submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Computer Engineering

Summer 2015



DESIGN AND CHARACTERIZATION OF A MIXED-SIGNAL PCB

FOR DIGITAL-TO-ANALOG CONVERSION

IN A MODULAR AND SCALABLE INFRARED SCENE PROJECTOR

by

Jacob Benedict

Approved: _____

Fouad Kiamilev, Ph.D.
Professor in charge of thesis on behalf of the Advisory Committee

Approved: _____

Kenneth E. Barner, Ph.D.
Chair of the Department of Electrical and Computer Engineering

Approved: _____

Babatunde A. Ogunnaike, Ph.D.
Dean of the College of Engineering

Approved: _____

James G. Richards, Ph.D.
Vice Provost for Graduate and Professional Education

ACKNOWLEDGMENTS

I would like to thank a number of people for making this work possible. First I would like to thank Dr. Kiamilev for the opportunity to work on the research described in this thesis. As my advisor, Dr. Kiamilev has demonstrated what it means to be a strong leader by giving direction without limiting the personal expression and ideas of others.

Additionally, I would like to thank the members of CVORG whose staggeringly massive collective intelligence has made my time as a graduate student the most enlightening years of my life. Each one of you, in some way, has contributed to my growth as an engineer, without which, this thesis would not be possible. I would like to particularly thank Josh Marks who designed the first version of the FMC 4DAC board and served as a wealth of information during my redesigns for versions two and three.

Last, but certainly not least, I would like to thank my family. Without the love and support of my parents and the values they instilled in me I would not be the person I am today. I also owe a huge part of my success to my remarkable wife, Christine, whose unwavering support and love propels me forward each day.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Infra-red (IR) sensors have proven instrumental in a wide variety of fields from military to industrial applications. The proliferation of IR sensors has spawned an intense push for technologies that can test and calibrate the multitudes of IR sensors. One such technology, IR scene projection (IRSP), provides an inexpensive and safe method for the testing of IR sensor devices.

Previous efforts have been conducted to develop IRSPs based on super-lattice light emitting diodes (SLEDS). A single-color 512x512 SLEDs system has been developed, produced, and tested as documented in Corey Lange's Master's thesis, and a GOMAC paper by Rodney McGee [1][2]. Current efforts are being undergone to develop a two-color 512x512 SLEDs system designated (TCSA).

The following thesis discusses the design and implementation of a custom printed circuit board (PCB), known as the FMC 4DAC, that contains both analog and digital signals. Utilizing two 16-bit digital-to-analog converters (DAC) the purpose of the board is to provide four analog current output channels for driving the TCSA system to a maximum frame rate of 1 kHz. In addition, the board supports a scalable TCSA system architecture. Several copies of the board can be run in parallel to achieve a range of analog channels between 4 and 32.

Chapter 1

INTRODUCTION

1.1 Background

Infra-red (IR) sensors have proven instrumental in a wide variety of fields from military to law enforcement and industrial applications. IR imaging systems are complex, sensitive, and expensive devices that require frequent testing and calibration. Accurately verifying the operation of complex and highly integrated IR sensors is an equally complex task to complete. Infra-red scene projectors (IRSP) are IR sources that are capable of real-time testing of IR imaging systems. These IRSPs generate an accurate two-dimensional infra-red scene, which is read by IR sensors as real-time IR signatures. Infra-red scene projectors provide an inexpensive method for reliably calibrating infra-red imaging systems without the risk of damage to system components.

IR scene projector and sensor technologies operate in the infra-red spectrum, which extends from wavelengths of .75 to 1,000 microns. A large concentration of IR sensors and IRSPs operate in a spectral range referred to as mid-wave IR (MWIR), which consists of a range from 3 to 5 microns. One such IRSP technology capable of emitting in the MWIR range consists of fabricating emitter arrays using MEMS thermal resistors. Since the 1980s, the dominant IRSP technology in use has been the thermal resistor arrays. A number of limitations exists for resistor arrays including: apparent temperature limited to actual temperature (<700K); poor fill-factor; poor performance when simulating very cold targets; and the inability to emulate a non-

black-body spectrum [3, 4, 5, 6]. However, recent research and development of IR-LED based infra-red scene projectors has altered the IRSP landscape. LED based IRSPs hold the potential to replace current technologies due to their faster frame rates, higher temperature scenes, and higher density yielding higher spatial resolution [7][8].

The world's first infra-red LED scene projector is the results of a collaboration between CVORG, at the University of Delaware, and the University of Iowa's research group led by Professor Thomas Boggess. This first of its kind IRSP utilizes a new projector technology called Super Lattice LEDs (SLEDs). Since its conception a complete SLEDs IRSP system has been designed, fabricated, and evaluated at many user facilities. The end result is a robust IR projector with a resolution of 512x512 and frame rate of 100Hz [9].

1.2 Motivation

A joint research project continues between the University of Delaware and the University of Iowa to develop the next generation SLEDs infra-red scene projector. This new research project aims to increase the achievable dynamic range of the projector by having two drive transistors of different drive strengths per pixel. Because this new projector will have two emission intensities per pixel the new system is called Two-Color SLEDs Array (TCSA). There are other advancements being made with the second generation SLEDs projector which include adding signal termination for the Read-In Integrated Circuit (RIIC) I/O signals, frame transitions, advanced NUC, and increasing the number of analog channels [2]. The work discussed in this paper is a critical piece of our approach to increasing the number of analog channels for the TCSA IRSP.

Chapter 2

PREVIOUS WORKS 512x512, 100Hz SINGLE COLOR SLEDS IRSP

The single-color first generation SLEDs projector is a complete system that has been constructed and has thousands of hours of operation. The system is designed to read in a single-link DVI input from a scene generator and display that image on the SLEDs array. Two of the three 8-bit color channels from the DVI input are merged to form a 16-bit monochromatic image. This image is decoded into quadrants and output to the RIIC. Pixel addressing is controlled by digital addressing lines, and pixel intensity is set using analog lines. The critical components of the system are discussed in more detail below.

2.1 RIIC

A SLEDs RIIC consists of a CMOS ASIC fabricated using the C5N process by On Semiconductor. The RIIC contains a two dimension array of 512x512 pixels with each unit pixel occupying a 48x48 micron pitch cell. A single pixel includes one drive transistor for creating a voltage controlled current source, circuitry for x and y coordinate addressing, and transistors dedicated to pixel testing [10]. The RIIC is flip chip bonded to the SLEDs array to form what is called an emitter hybrid or SLEDs hybrid.

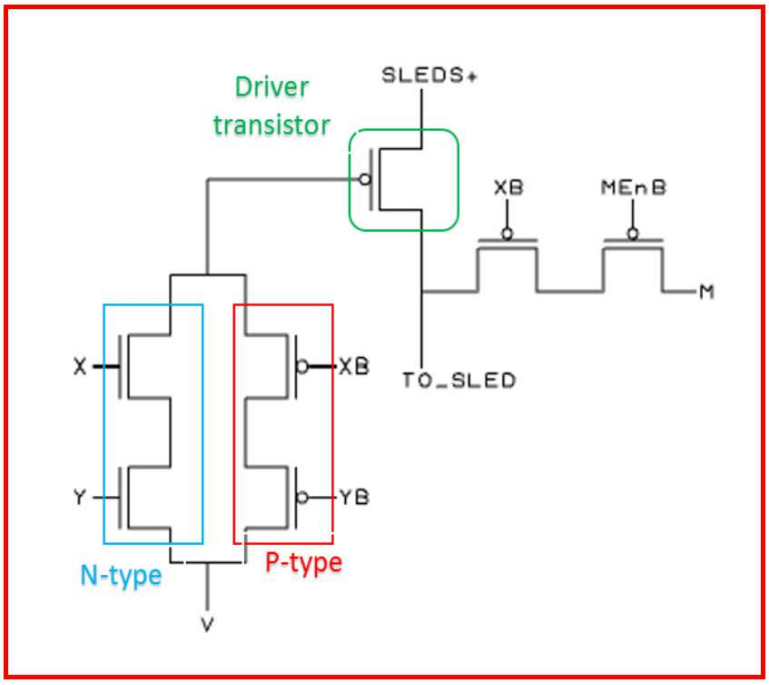


Figure 2.1 Single pixel schematic

2.2 SLEDs Array

The SLEDs arrays are fabricated using MBE growth on a gallium antimonide (GaSb) substrate. Alternating layers of indium arsenide (InAs) and GaSb, known as super-lattices, are grown on top of the substrate with atomic precision. The InAs/GaSb super-lattices form active regions and are separated by tunnel junctions. Changing the emission wavelength of the SLEDs array is possible through bandgap engineering, which is done by altering the thickness of layers in the super-lattice growths [11]. After growth, the SLEDs wafers are etched using photolithography to produce individual pixels. Anode and cathode contacts are added to each pixel using metal deposition, so the array can connect to the RIIC. Indium bumps are deposited on each contact of the SLEDs array and RIIC and then the two are pressed together to form a

complete SLEDs hybrid, shown in Figures 2.3 and 2.4 [12]. The SLEDs hybrids are then mounted in a liquid nitrogen filled Dewar for cooling the SLEDs to 77 degrees Kelvin.

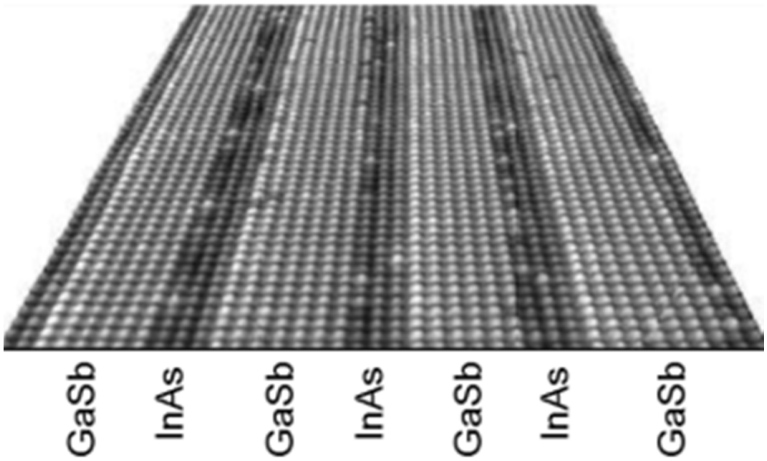


Figure 2.2 STM cross sectional image of InAs/GaSb SLEDs super-lattice growth

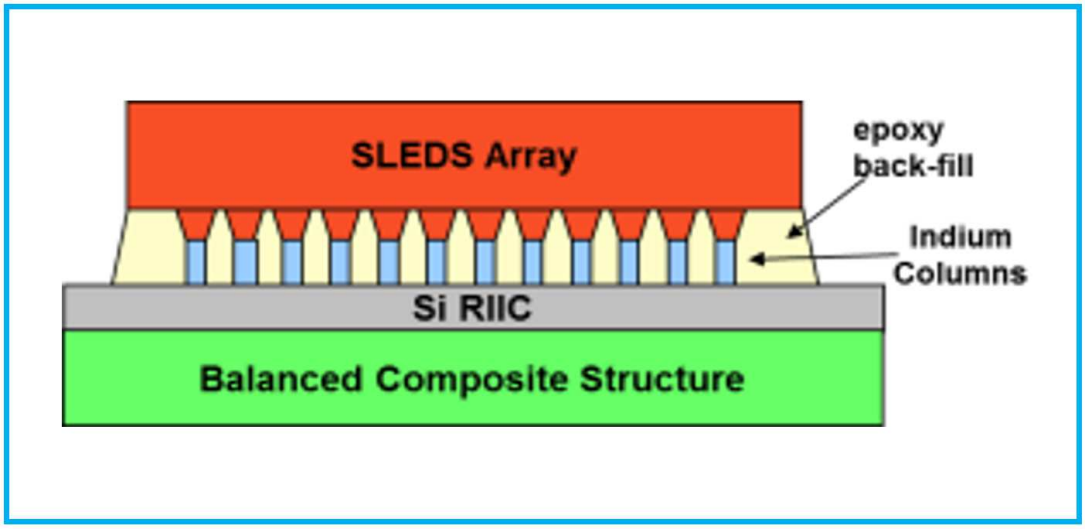


Figure 2.3 SLEDs hybridization using flip chip method

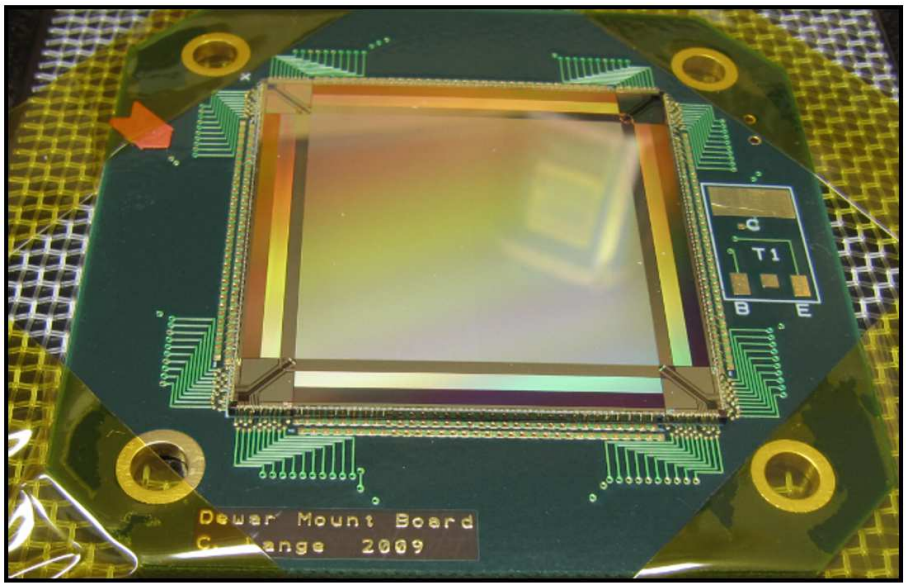


Figure 2.4 Hybridized SLEDs array on carrier board

2.3 Close Support Electronics

Close Support Electronics (CSE) perform the task of interfacing the scene generator to the RIIC. Merging the DVI input into a monochromatic image, decoding the image into quadrants, non-uniformity correction, digital addressing lines, and analog lines are all performed by the amalgamation of components that make up the CSE. The CSE consists of the FPGA, AD9747 Evaluation board (DAC Eval board), Analog Amplifier (DAC Amp), and Interface board. More detail on each component of the CSE is provided below.

2.3.1 FPGA

FPGAs, which stands for Field Programmable Gate Array, have experienced a rampant adoption throughout the electronics industry. Their wide acceptance is due to the FPGA's ability to be programmed thousands of times and because it can be

quickly configured into a virtually unlimited number of circuits [13]. SLEDs CSE utilizes Xilinx's ML605 equipped with a Virtex-6 XC6VLX240T FPGA chip. The ML605 gives us the ability to programmatically drive hundreds of digital signals based on our desired output. DVI input from the scene generator is received by a DVI I/O FMC module that interfaces with the low pin count (LPC) FMC connector on the ML605 (FMC Slot#1 in Figure 2.5). The FPGA merges the DVI input into a 16-bit monochromatic image which is then pushed to the RIIC for display on the SLEDs array. FMC Slot#2 is a high pin count (HPC) FMC slot that breaks out signals to both the Interface board and AD9747 Evaluation boards. The ML605 sends 16 digital addressing lines to the interface board, as well as I^2C communication, and two 16-bit values to the DAC Eval board for controlling the analog lines. An in depth description of the functions provided by the ML605 can be found in Kassem Nabha's Master's thesis [9].

Figure 2.5 ML605 FPGA

2.3.2 AD9747 Evaluation Board

An off the shelf board, the AD9747 Evaluation board contains one AD9747 dual DAC chip manufactured by Analog Devices. The DAC chip can be programmed into any of its various operating modes through a USB interface with a computer running specialized software from Analog Devices. A clock source and two 16-bit digital values are provided by the ML605. From the 16-bit value the AD9747 produces a corresponding slew current output with a full scale current of 31.7 mA at 250MHz. In order to reach the target frame rate of 100Hz, SLEDs requires 4 analog channels; therefore, we use two DAC Eval boards. With four channels the SLEDs array is broken into four quadrants, each with its own analog channel. As mentioned in section 2.1, a SLEDs pixel is voltage controlled, so the four DAC output channels are sent across shielded SMA cables to a trans-impedance amplifier for converting the current into suitable voltage signals.

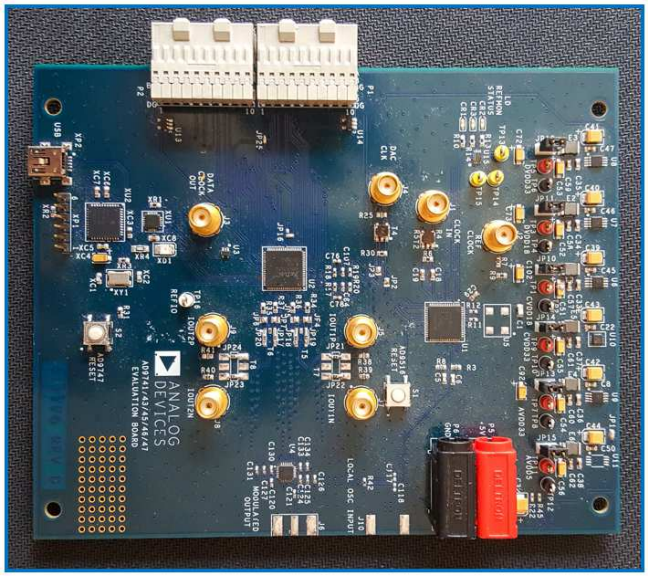


Figure 2.6 DAC Eval board

2.3.3 Analog Amplifier

Our team designed and built a custom trans-impedance amplifier, shown in Figure 2.7, to meet the high speed, low-noise voltage signal criteria required by the pixel circuitry. The design uses a TH6012 op-amp from Texas Instruments capable of current feedback, high slew rates, and low total harmonic distortion. Each current output channel from the DAC Eval board is amplified to its corresponding voltage value, with a steady 10V output being the lowest scale and a square wave with a swing of 0V to 10V being full scale. We used an inverting configuration with the output providing a tunable feedback impedance to the negative input pin for adjusting amplifier gain. To account for the highly capacitive load of the SLEDs hybrid the design has a tunable RC snubber for output edge damping [14]. Each channel from the DAC Amp is transmitted across a separate SMA cable to the Interface board.

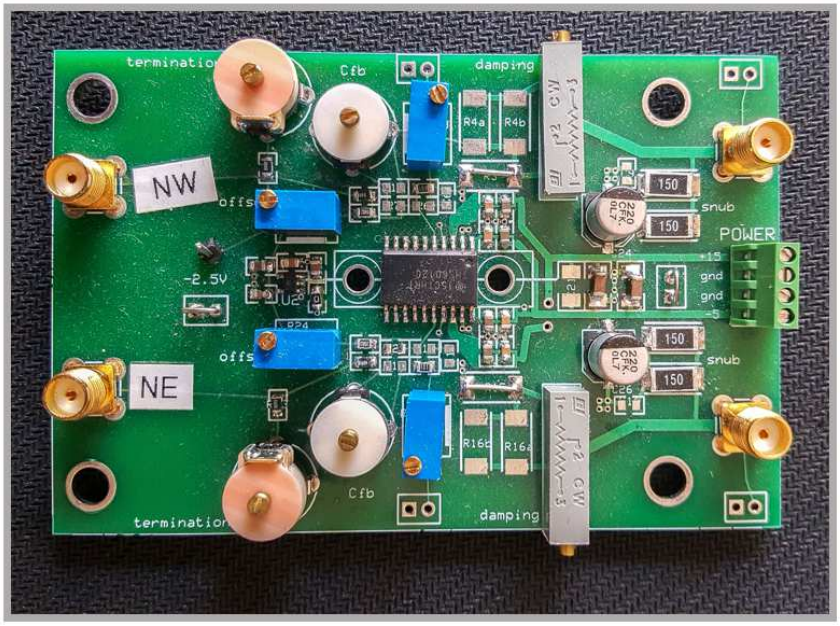


Figure 2.7 DAC Amp board

2.3.4 Interface Board

The SLEDs Interface board serves the instrumental role of feeding the RIIC with the multitude of signals being produced by the various CSE components. Power for the Interface board can be a 10V to 12V source, which is distributed or converted for powering the RIIC, DAC Evaluation boards, and DAC Amps. Digital address lines from the ML605 are level shifted on the Interface board from 2.5V to the 5V logic needed by the RIIC. The ML605 also communicates through I^2C with the Interface board to control a circuit breaker that serves to limit the current draw of the SLEDs hybrid chip based on a User software defined limit. Four SMA cables bring in the analog lines from the DAC Amps. All of these signals, along with system ground, are routed to four 34-pin connectors that are interfaced via ribbon cables to the Dewar that holds the RIIC and SLEDs array.

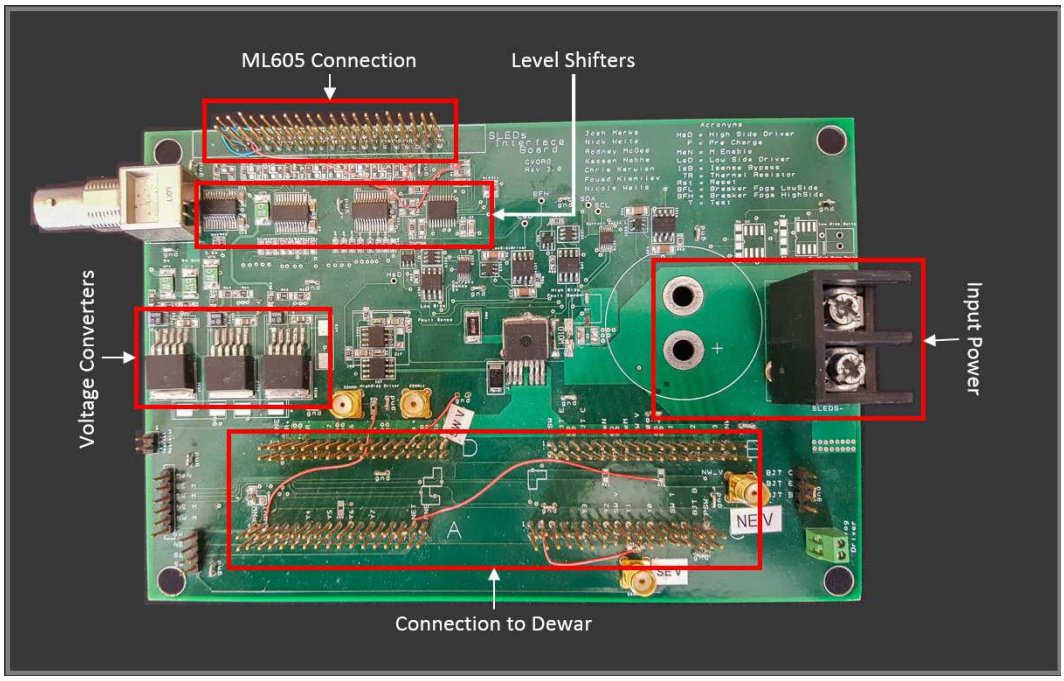


Figure 2.8 Interface board

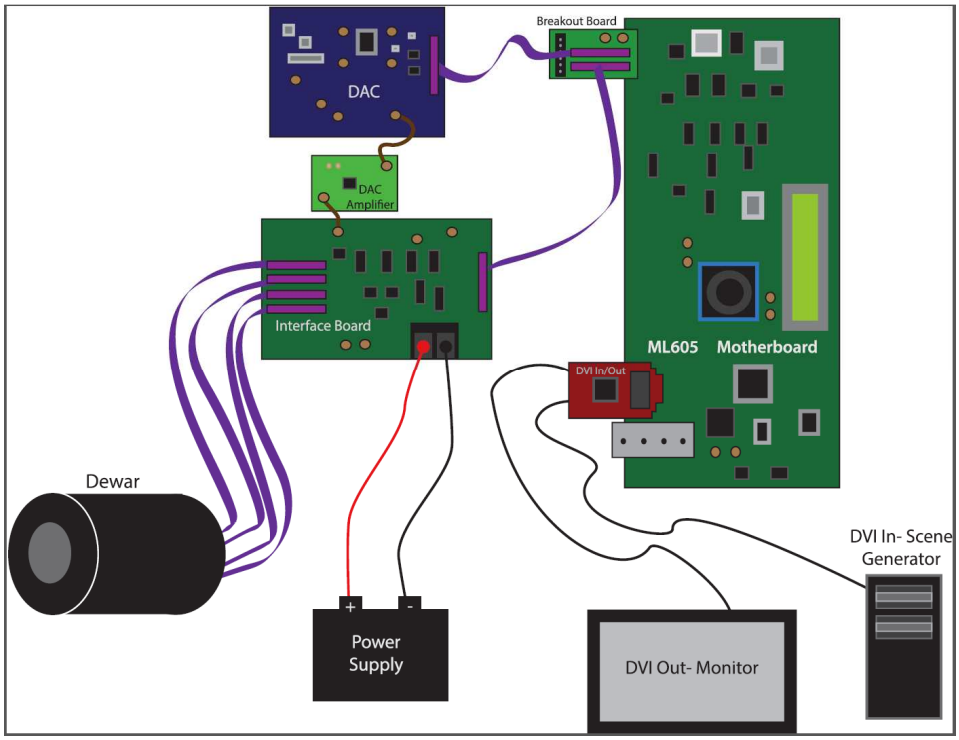


Figure 2.9 Hardware architecture of 100Hz SLEDs system

2.4 System Performance

Project goals for the 100Hz SLEDs system were to have a packaged IRSP capable of displaying IR scenes at a frame rate of 100Hz. Rigorous testing validated our efforts with the SLEDs system logging hundreds of hours of operation drawing IR scenes at 100Hz. However, testing did reveal certain limitations with the 100Hz SLEDs system. When drawing low intensity IR scenes, the oversized power transistor within the pixels causes noise to dominate its output, thereby reducing dynamic range. In addition, 100Hz was only an intermediary goal on a path to a 1 kHz system. Under a new research project, TCSA, efforts are ongoing to redesign the system to have two-stage transistor drive circuitry in the pixel for improving dynamic range, and additional analog lines for achieving 1 kHz. A more detailed description of the 100Hz

SLEDs system can be found in Rodney McGee's paper "512x512, 100Hz Mid-wave Infrared LED Scene Projector" submitted to GOMAC in 2015 [2].

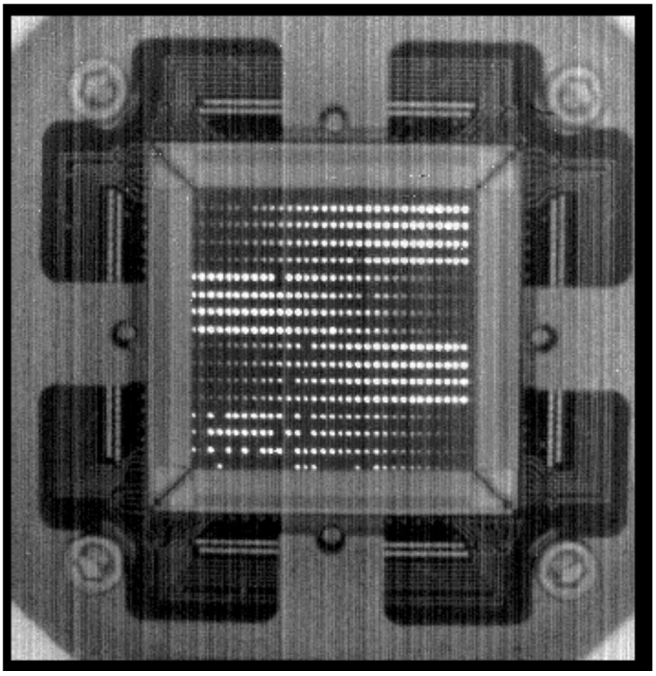


Figure 2.10 Sparse Grid pattern on 100Hz SLEDs system

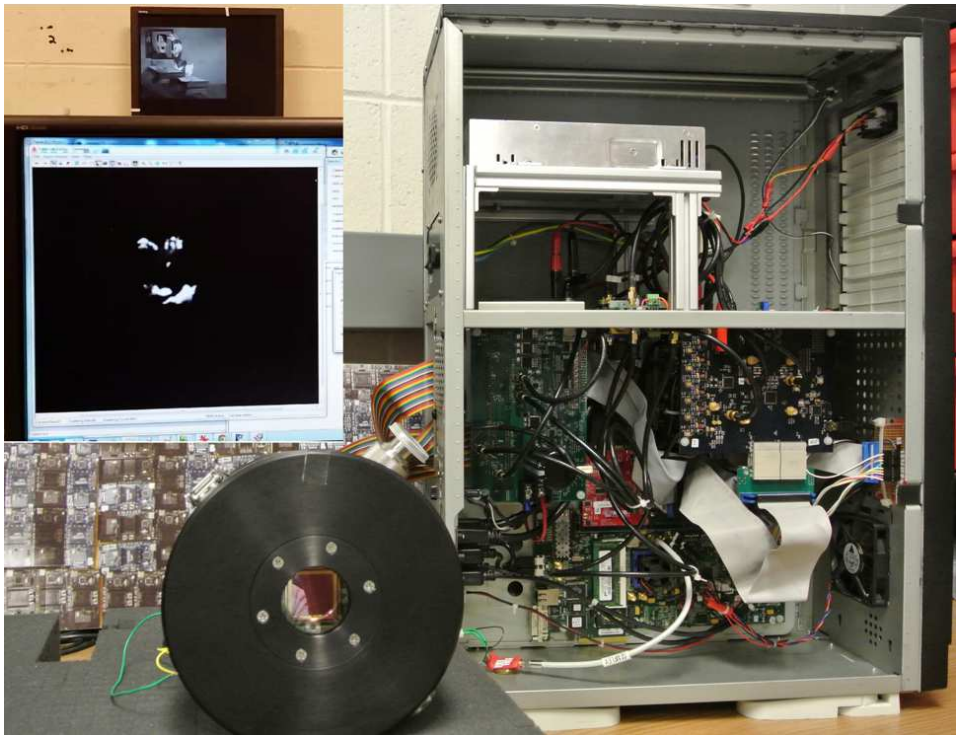


Figure 2.11 CSE for current generation 512x512 system. Inset: Donald Duck in “Der Fuehrer's Face” (1943 Disney Pictures and RKO Radio) (Top) displayed on the projector and captured with an IR camera (Bottom).

Chapter 3

CURRENT WORKS 1 kHz TWO COLOR SLEDS IRSP

As discussed in section 1.2, the TCSA research project is a continuation of SLEDs IR scene projection technology. The goals for TCSA focus on improving system performance and advancing the capabilities of SLEDs technology. Most of the components from the 100Hz SLEDs system have been redesigned to achieve the desired system performance. The RIIC and SLEDs array have been redesigned to incorporate a second drive transistor as well as some additional features. All of the CSE components have new designs to meet the higher 1 kHz frame rate goal.

3.1 RIIC and TCSA Array

In the 100Hz SLEDs RIIC pixel, a single large PMOS transistor drives the SLEDs. For low apparent temperature scenes (such as 300K) the PMOS transistor is simply too big to achieve the few microamperes needed. Solving this limitation requires a RIIC with two parallel-connected transistors per pixel keeping within the same 48x48 micron pitch. Milliamp drive currents are supplied by a large transistor and micro-amp drive strengths are supplied by a smaller transistor [15]. Other improvements include in-pixel CMOS address logic, an increase of analog DAC drive channels from 4 to 32, serial control mode, and 50 Ohm termination of external analog and digital lines. Currently, a 32x32 TCSA RIIC has been fabricated and is undergoing testing to verify correct operation before a full 512x512 RIIC is fabricated.

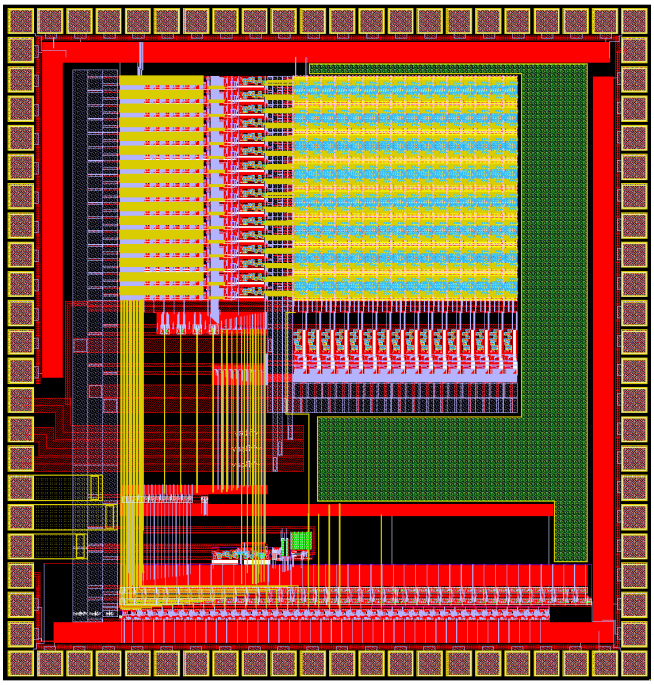


Figure 3.1 16x16 TCSA RIIC layout

The University of Iowa designed and fabricated a new two-color SLEDs arrays. A single TCSA pixel still occupies a 48x48 micron pitch, but has two different super-lattice structures each tuned to a different wavelength. Each color has its own anode contact and both share a common cathode contact increasing the number of contacts from two to three for the TCSA arrays. Separate anode contacts means the emission of each color are independently controlled. Current testing shows the emission wavelengths of the TCSA array to be 3.8 µm for “blue” MWIR and 5 µm for “red” MWIR [16].

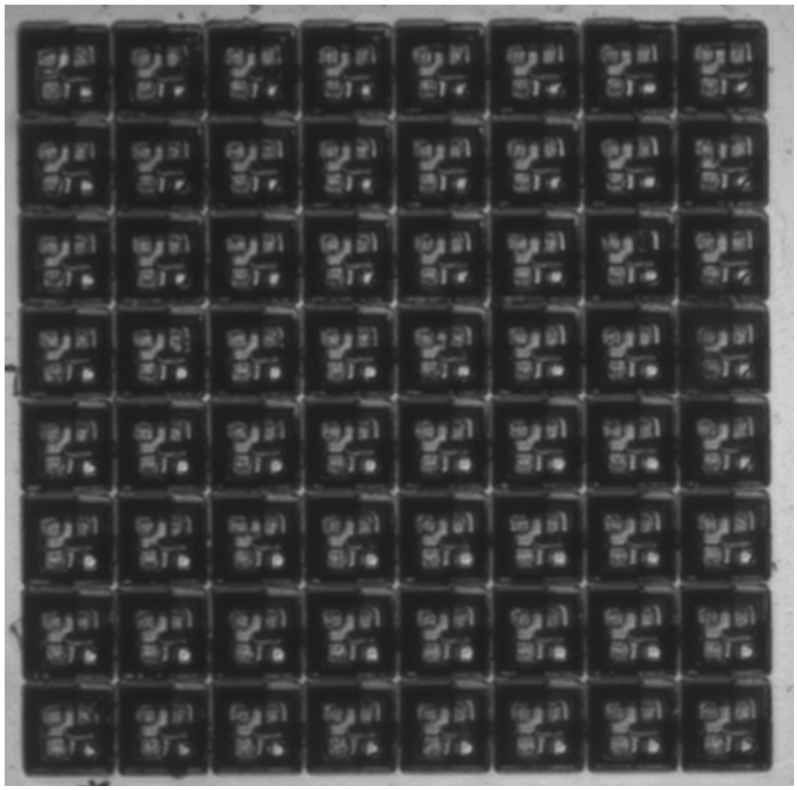


Figure 3.2 Fully processed 8x8, 48 µm pitch, TCSA array with indium bumps

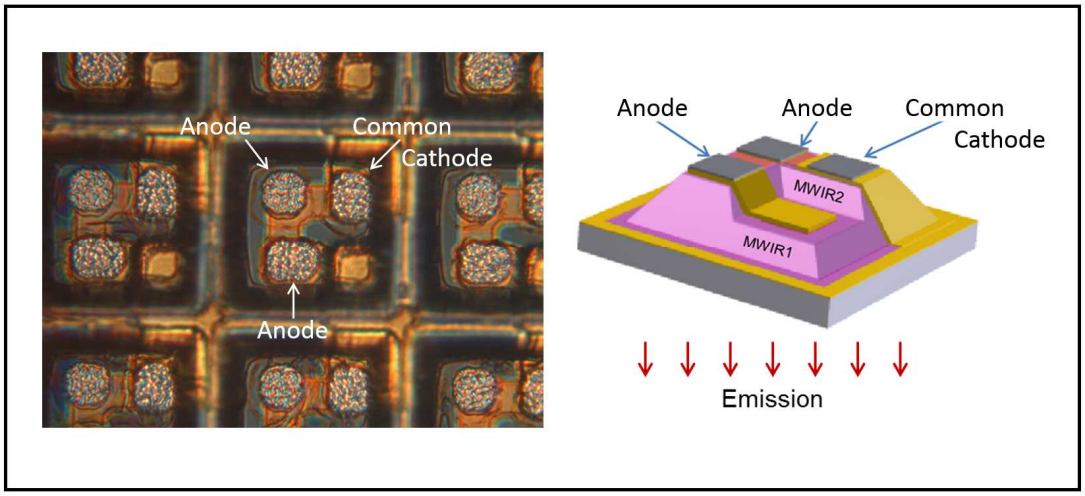


Figure 3.3 Expanded view of Figure 3.2 (left) and TCSA pixel layout (right)

3.2 Close Support Electronics

All of the CSE components for the TCSA system are being redesigned, built, and tested to satisfy the performance criteria set forth for the project. A new FPGA has been chosen to expand system resources to meet the signal density needed by the new system. The CSE architecture has changed to be more modular to allow for easy scalability as displayed in Figure 3.8. The latest designs for the TCSA CSE are described in the following sections.

3.2.1 FPGA

With only two FMC connectors, the ML605 lacks the resources required by the TCSA system. An Inrevium TB-6V-LX760-LSI (TB6) motherboard equipped with a Virtex-6 LXT760 FPGA has replaced the ML605 in the TCSA system. The LX760 has more than three times as many logic cells as the ML605's LX240T, as well as more configurable logic blocks [17]. Table 3.1 shows a summary of the features for the LX760 and LX240T FPGAs. The TB6 also has more memory than the ML605, allowing for the development of larger projects [18]. The TB-6V-LX760-LSI supports ten LPC FMC expansion slots, which are crucial to the scalability to a 1 kHz frame rate. Future plans to scale the system to higher frame rates and larger array sizes are also satisfied by the increased available resources of the TB-6V-LX760-LSI.

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices(2)	Block RAM Blocks			MMCMs(4)	Interface Blocks for PCI Express	Ethernet MACs(5)	Maximum Transceivers		Total I/O Banks(6)	Max User I/O(7)
		Slices(1)	Max Distributed RAM (Kb)		18 Kb(3)	36 Kb	Max (Kb)				GTX	GTH		
XC6VLX75T	74,496	11,640	1,045	288	312	156	5,616	6	1	4	12	0	9	360
XC6VLX130T	128,000	20,000	1,740	480	528	264	9,504	10	2	4	20	0	15	600
XC6VLX195T	199,680	31,200	3,040	640	688	344	12,384	10	2	4	20	0	15	600
ML605 → XC6VLX240T	241,152	37,680	3,650	768	832	416	14,976	12	2	4	24	0	18	720
XC6VLX365T	364,032	56,880	4,130	576	832	416	14,976	12	2	4	24	0	18	720
XC6VLX550T	549,888	85,920	6,200	864	1,264	632	22,752	18	2	4	36	0	30	1200
TB6 → XC6VLX760	758,784	118,560	8,280	864	1,440	720	25,920	18	0	0	0	0	30	1200
XC6VSX315T	314,880	49,200	5,090	1,344	1,408	704	25,344	12	2	4	24	0	18	720
XC6VSX475T	476,160	74,400	7,640	2,016	2,128	1,064	38,304	18	2	4	36	0	21	840
XC6VHX250T	251,904	39,360	3,040	576	1,008	504	18,144	12	4	4	48	0	8	320
XC6VHX255T	253,440	39,600	3,050	576	1,032	516	18,576	12	2	2	24	24	12	480
XC6VHX380T	382,464	59,760	4,570	864	1,536	768	27,648	18	4	4	48	24	18	720
XC6VHX565T	566,784	88,560	6,370	864	1,824	912	32,832	18	4	4	48	24	18	720

Table 3.1 Virtex-6 FPGA feature summary [17]

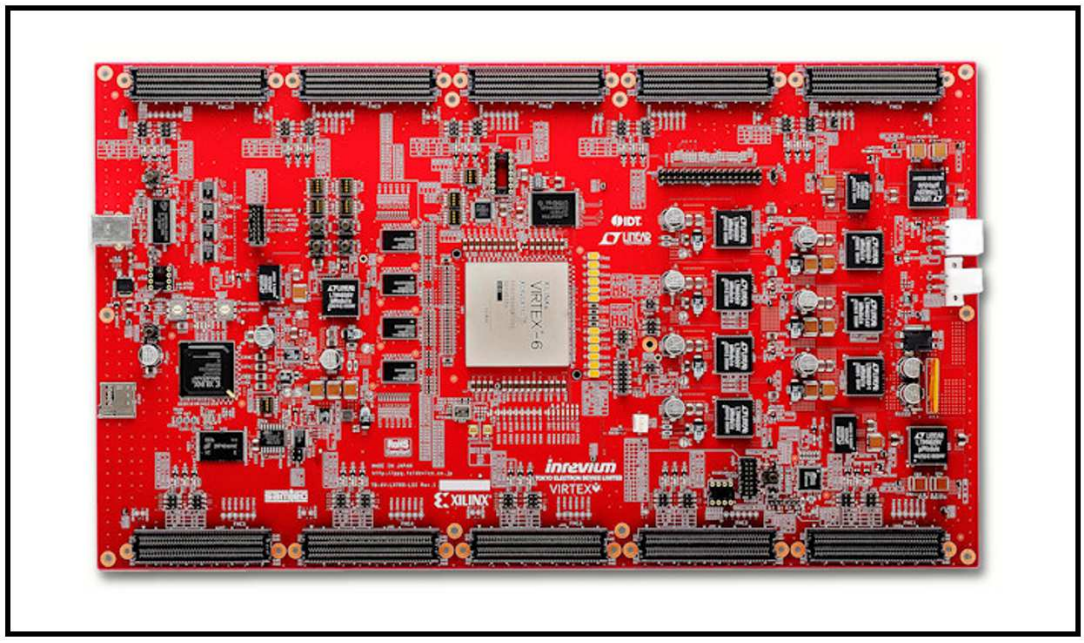


Figure 3.4 TB-6V-LX760-LSI board

3.2.2 Interface Board

The new Interface board provides signal routing from the CSE to the RIIC and power distribution for multiple system components. One Interface board has enough slots to fit four DAC Amp boards, which gives a total of 16 analog lines per Interface board. Four IDE cables provide a 200 pin (100 signal/power and 100 ground) connection to the RIIC. To reduce ringing and signal settling delays on many of the analog and digital lines all signals are routed using 100-ohm impedance matched traces. The traces are routed over a ground plane with ground shields routed between signals to reduce crosstalk as pictured in Figure 3.6. Power supplies for the DAC Amp and RIIC are supplied by the Interface board. These power supplies are all filtered through linear supplies with extra filtering for high sensitivity supplies [19]. The board is configurable between the requirements of the current generation two-color system and future generation large-format one-color systems. An on-board microcontroller monitors the voltages and currents of the main power rails and displays them on an LCD. It also monitors fan speeds and performs other ancillary functions. For applications where more than 16 analog channels are needed, the Interface board can provide/accept the main power rails to/from another copy of itself such that each set of 4 DAC Amps (one side of an SFPGA worth) use a separate copy of the Interface board.

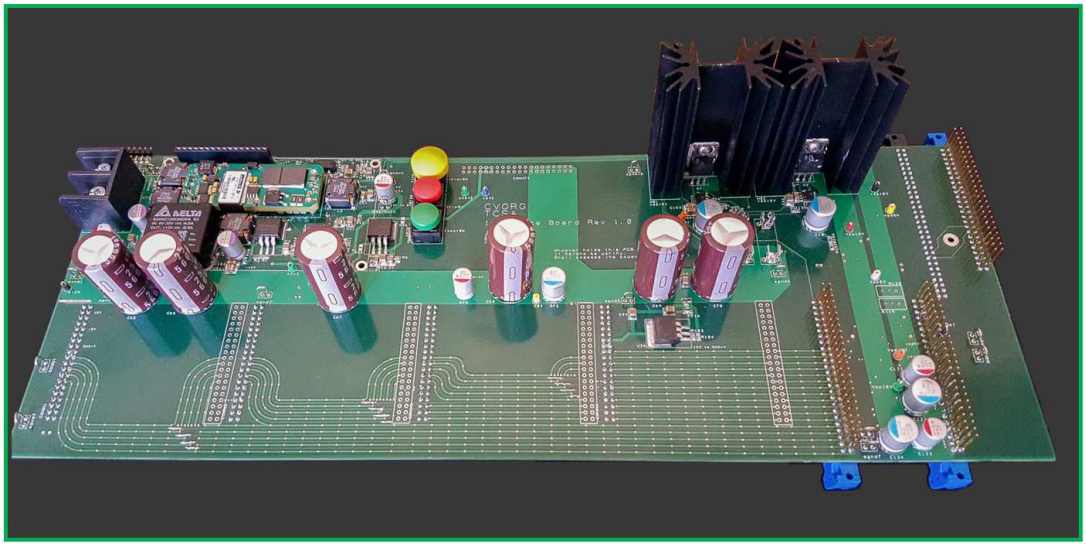


Figure 3.5 TCSA Interface board

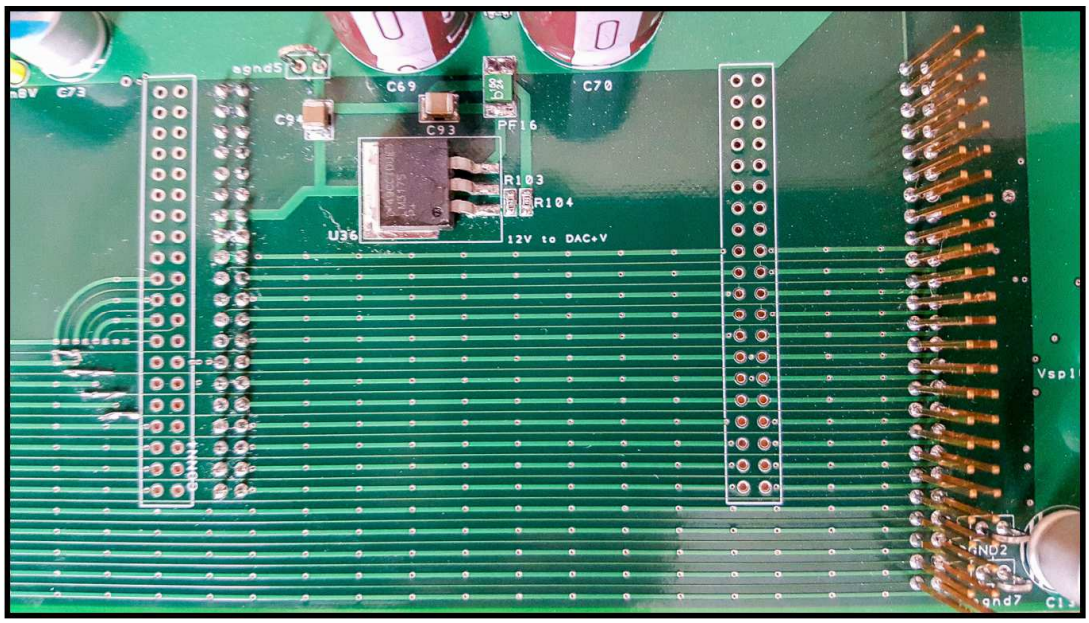


Figure 3.6 Impedance matched trace routing scheme

3.2.3 DAC Analog Amplifier

The original circuit design for the DAC Amp from the 100Hz system remains virtually unchanged; however, instead of only supplying two analog output channels, four channels are output from a single DAC Amp board by using two THS6012 amplifiers per board. All analog outputs from the amplifiers are fed back to an analog-to-digital converter and microcontroller on the FMC 4DAC board to monitor the signals. Future plans are to put programmable variable resistors on the DAC Amp board to tune the outputs of the amplifiers based on the fed back signals. In the TCSA system, the DAC Amp plugs directly into the Interface board and FMC 4DAC board, eliminating the need for SMA cables. Currently, the DAC Amps are designed for single-ended operation, but a redesign of the circuit to amplify differential pairs from the FMC 4DAC is planned for future works.

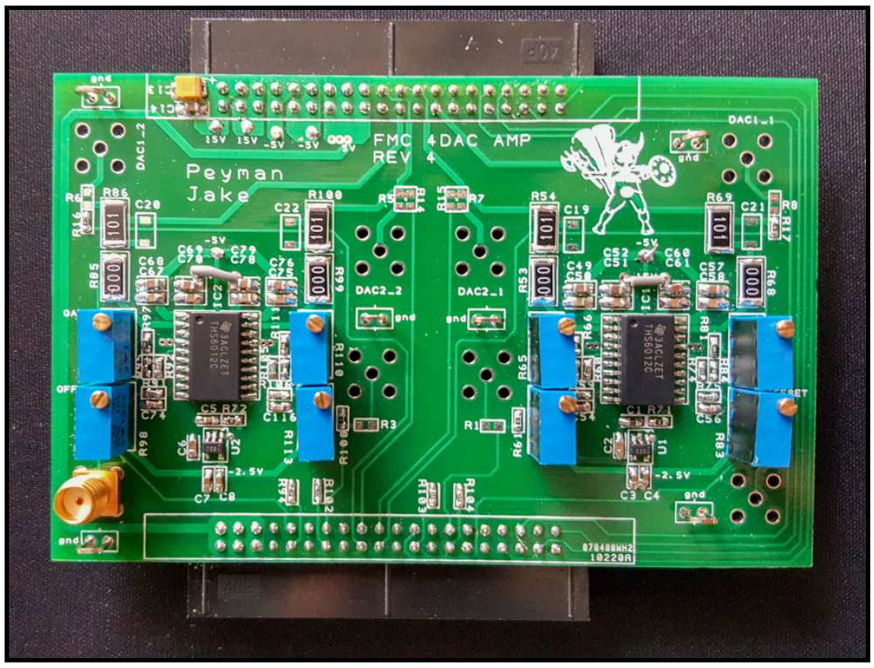


Figure 3.7 TCSA DAC Amp

3.2.4 4 Channel DAC Board

The AD9747 Evaluation board has been replaced by a custom designed, 4 channel current output DAC board designated as FMC 4DAC board. Whereas the Eval board only has one two-channel DAC, a single FMC 4DAC contains two DAC chips for a total of four analog outputs per board. The FMC 4DAC receives four 16-bit values, two 16-bit values per DAC chip for each channel. All four digital values are converted to corresponding current values by the AD9747. These four current signals are sent to the DAC Amp board for amplification. The remainder of this thesis is dedicated to explaining the design, implementation, and testing of the FMC 4DAC board.

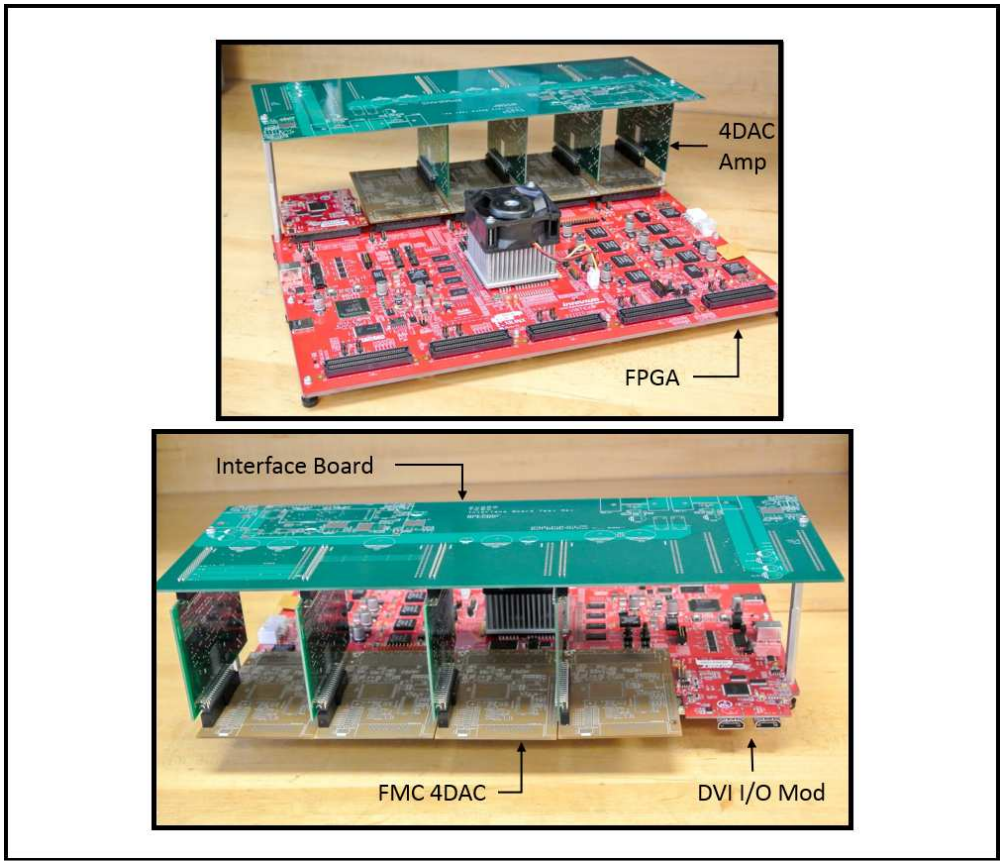


Figure 3.8 TCSA CSE architecture

Chapter 4

CUSTOM, 4 CHANNEL CURRENT OUTPUT DAC DESIGN

As previously mentioned in Chapter 3, the project objectives of the TCSA IR scene projector are a two color system capable of frame rates up to 1 kHz. Achieving these objectives required a new design for the RIIC. The new design has increased the number of input analog channels on the RIIC from 4 to 32. By increasing the number of analog channels, each channel is responsible for assigning values to fewer pixels. With fewer pixels to address, each channel can write its subset of pixels faster, thereby increasing the overall frame rate of the projector. In order to supply the many analog channels for the TCSA system a board had to be designed for the CSE.

The SLEDs 100Hz system has four analog channels that are supplied by the AD9747 Evaluation boards. Each DAC Eval board has two channels, so two DAC Eval boards are used in the CSE for the 100Hz projector. Generating the 32 channels needed to run the TCSA system would require 16 DAC Eval boards, which would make the system CSE too large and complicated. Instead, we designed our own board using the same AD9747 DAC chip. With two DAC chips per board supplying four analog channels, only eight boards are required to reach thirty two channels providing easy scalability of the TCSA architecture. The new design has been given the designator FMC 4DAC and will be referred to as such for the remainder of this paper.

4.1 Circuit Description

4.1.1 Digital-to-Analog Converter

The FMC 4DAC is designed around Analog Devices' AD9747 dual digital-to-analog converter. According to the datasheet, the AD9747 has a 16-bit resolution and a max clock frequency of 250MHz [20]. The DAC has its own internal 1.2V precision reference voltage source, so the need for an external reference voltage source is eliminated. It requires four power supplies for operation: 1.8 CVDD (clock supply), 1.8 DVDD, 3.3 DVDD, and 3.3 AVDD.

A Serial Peripheral Interface (SPI) port gives the ability to read and write to registers on the DAC that configure it for certain modes of operation. The most important of these registers are the Data Control, DACx Gain, and SPI Control registers. Writing to the Data Control register configures the input data as twos complement binary format or unsigned binary format. This register also controls whether the chip is in two port mode where both DAC channels receive their own digital input port, or in single port mode where both channels share a single port and the data is interleaved and steered toward the respective DAC. The DACx Gain registers configure the full-scale current for the analog outputs with 8.6 mA being the minimum and 31.7 mA being the maximum value. Each on-chip DAC has its own DAC Gain register, so their full-scale outputs can be set to different levels. The SPI Control register controls whether communication to the DAC is done using 4-wire SPI mode or 3-wire mode, and whether the first bit of the incoming data is the LSB or MSB. All of the registers can also be reset to their default values with a single bit in the SPI Control register. With careful timing considerations the AD9747 can even be reconfigured mid-communication cycle.

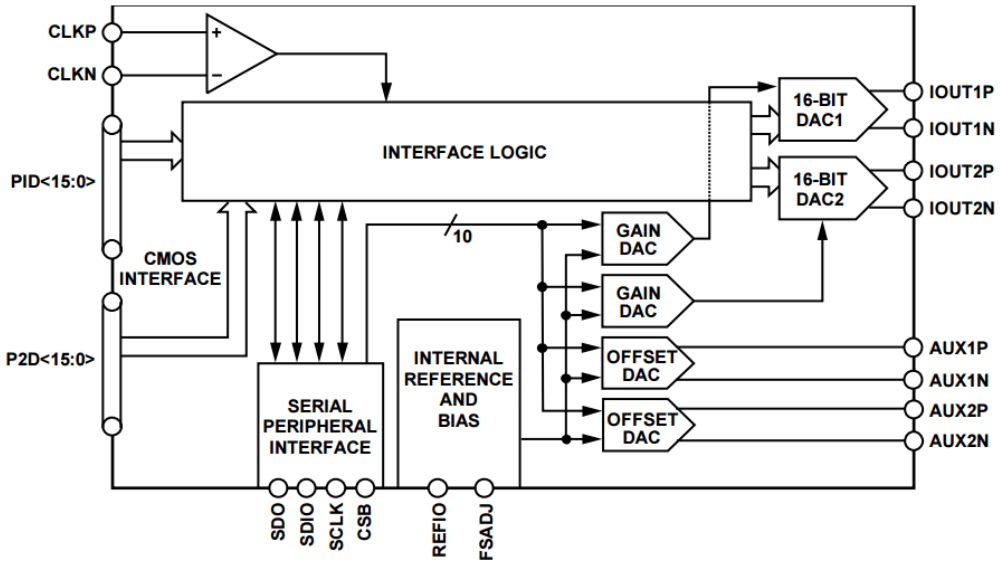


Figure 4.1 Functional block diagram for AD9747 [20]

Parameter	AD9745 Min	AD9745 Typ	AD9745 Max	AD9746 Min	AD9746 Typ	AD9746 Max	AD9747 Min	AD9747 Typ	AD9747 Max	Unit
RESOLUTION		12			14			16		Bits
ACCURACY										
Differential Nonlinearity (DNL)		±0.13			±0.5			±2.0		LSB
Integral Nonlinearity (INL)		±0.25			±1.0			±4.0		LSB
MAIN DAC OUTPUTS										
Offset Error		±0.001			±0.001			±0.001		%FSR
Offset Error Temperature Coefficient		0.1			0.1			0.1		ppm/°C
Gain Error		±2.0			±2.0			±2.0		%FSR
Gain Error Temperature Coefficient		100			100			100		ppm/°C
Gain Matching (DAC1 to DAC2)		±1.0			±1.0			±1.0		%FSR
Full-Scale Output Current	8.6		31.7	8.6		31.7	8.6		31.7	mA
Output Compliance Voltage	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	V
Output Resistance		10			10			10		MΩ

Table 4.1 Specifications of AD9747 [20]

In our design both AD9747s are configured for dual-port mode and input data of the unsigned binary format. All four DAC outputs are set to their maximum full-scale current of 31.7 mA. Initializing the DAC registers is performed by an on-board microcontroller with SPI capabilities. Each DAC receives two 16-bit digital values within the range of 0 to 65535 for full scale. The four 16-bit digital values are sent by the FPGA and represent a light emission brightness level for a pixel in the TCSA projector. A value of zero on the digital inputs produces a current output of near zero, while a full scale value produces 31.7 mA at the output of the DAC. One analog output channel from the DAC consists of a differential pair (IOUT1P and IOUT1N in Figure 4.1). For our design only the positive output of each channel is used, because the DAC Amp is designed for single ended signals and not differential pairs.

Both DACs operate off the same differential clock pair provided by the FPGA. Their differential peak-to-peak voltage should be held between 800 and 1600 mV. Simple voltage divider networks on the FMC 4DAC board reduce the incoming 2.5 V clock pair to 400 mV each, producing a differential peak-to-peak voltage of 800 mV.

4.1.2 Microcontroller

An on-board microcontroller handles communication between components on and off the board and monitors power supplies. The 16-bit PIC24HJ256GP210A microcontroller from Microchip Technology is used on the most current version of the FMC 4DAC.

The PIC24's most important function is to provide SPI communication with the DACs. Using 4-wire SPI communication (SCLK, MOSI, MISO, and CS) the microcontroller interfaces with the DAC for configuring its registers. The PIC24 can also perform a software reset of the DACs using the SPI interface and a hardware reset

by momentarily pulling the reset pin on the DAC high. Upon power up, following the advice of the AD9747 datasheet, the PIC24 first pulses the reset pin high and then performs a software reset of the DACs. This process assures all registers are at their default values before any configuring of the DAC registers takes place.

Multiple analog pins on the PIC24 are dedicated to monitoring and controlling all four power supplies for the DACs. The digital and clock 1.8 V rails are fed directly into their respective analog pins, but the digital and analog 3.3 V supplies are voltage divided to 1.8 V to prevent overvoltage damage to the PIC24 analog pin circuitry. All DAC power supplies can be turned off at once via a single GPIO pin that is connected to a shutdown pin on each of the power rail's LDOs. If any power supplies fail the microcontroller can turn off all power to the DACs to prevent damage to the chip, as well as notify the User using status LEDs connected to the PIC24.

A second set of dedicated SPI pins on the PIC facilitate communication with an on-board analog-to-digital converter (ADC). As with the DACs, the microcontroller is responsible for configuring the ADC upon power up. The PIC24 also receives data from the ADC that needs to be analyzed as part of a feedback network from the DAC Amp board.

4.1.3 Analog-to-Digital Converter

Every analog channel output on the DAC Amp board must be hand-tuned via the potentiometers in its feedback networks. Performing this task is tedious and requires a lot of time. A scheme has been devised and implemented on the FMC 4DAC board that can potentially auto tune the analog channels through digital potentiometers. Output analog channels from the DAC Amp are fed back to the FMC 4DAC and into an ADC. The digital data from the ADC is sent to the PIC24

microcontroller for computation. Using I^2C communication pins the microcontroller sends commands to the digital capacitors, adjusting them until the analog outputs are properly tuned. Currently, only the circuitry on the FMC 4DAC has been implemented. A redesign of the DAC Amp board is in the near future and may see an addition of the digital capacitor circuitry.

4.1.4 FMC Connector

In the SLEDs 100 Hz system the DAC Evaluation board has DPG2 connectors for interfacing with other boards. Because the only connectors on the ML605 are FMC connectors multiple adapter boards are used to break out signal from one of the FMC connectors and route them to the DAC Eval board. Significant noise has been observed on the digital signals being fed to the DAC Eval board. We believe the noise to be a result of signal reflections at the many connector interfaces and noise coupled into the signals along their long path from the ML605 through unshielded ribbon cables. For this reason we moved away from the DPG2 connectors on the DAC Evaluation board and instead designed the FMC 4DAC to plug directly into the FMC slots on the FPGA. Moving to a direct FMC interface between the FMC 4DAC board and FPGA should theoretically reduce some of our signal integrity issues.

The FMC connectors are capable of high speed data transmission of up to 2 Gb/s with propagation delays of 158 ps or less, and a 3 dB insertion loss at 4 GHz (single-ended) [21][22]. The FMC 4DAC board uses a LPC FMC connector giving a 160 pin connection to the FPGA at a pitch of .05”. Signals on the 160 pins break down as follows:

- 64 single-ended digital signals for the DACs
- 4 single-ended data signals for the Interface board
- 1 differential clock pair for DAC clock input
- 1 dedicated UART serial communication pair
- 8 pins dedicated to power supplies from FPGA
- 62 digital grounds
- 18 unused (specialized pins from FPGA)

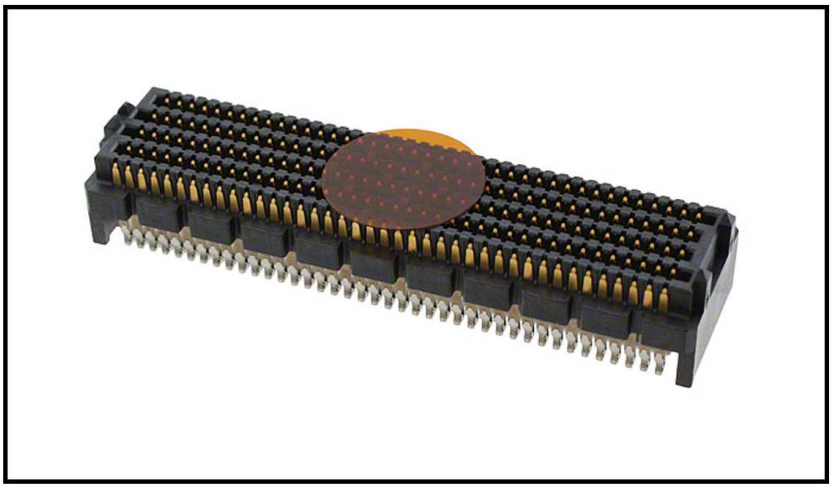


Figure 4.2 FMC connector (HPC version)

ITEM	TEST CONDITION	REQUIREMENT
LOW LEVEL CONTACT RESISTANCE (LLCR)	EIA-364-TP-23	Δ 10 mΩ maximum
INSULATION RESISTANCE (IR)	EIA-364-TP-21	> 25,000 MΩ minimum
DIELECTRIC WITHSTANDING VOLTAGE (DWV)	EIA-364-TP-20	900 VAC maximum
SIGNAL CONTINUITY	EIA-364-TP-87	No interrupts greater than 1 microsecond
CAPACITANCE	Test per EIA-364-30, All lines switching, with one victim bit.	Not to exceed 1.0 picofarad
CHARACTERISTIC IMPEDANCE	Test at 100ps RT(10%-90%)	100 +/-10% ohms - Diff 50 +/- 10% ohms - SE
CROSSTALK	Test at 100ps RT (10%-90%) All lines switching, with one victim bit.	5% of signal swing
PROPAGATION DELAY	Measurement made on line while others floating on mated connector	7mm stack - 67 ps 13mm stack - 158 ps
INSERTION LOSS (7 mm stack height rated @ -3 dB)	Mated Connectors Only (not including launches)	Single Ended - 4 GHz Differential Pair - 9 GHz

Table 4.2 FMC electrical performance [21]

4.2 Printed Circuit Board Design Implementation

Laying out the PCB design for the FMC 4DAC was done using Advance Circuits PCB Artist. Three versions (revisions) of the FMC 4DAC board have been designed and fabricated since the beginning of the TCSA program. Each of the three revisions are detailed below.

4.2.1 Version 1.0

Referred to as Rev1, our first design for the FMC 4DAC is an 8-layer board. Two layers are reserved for ground planes, three layers for power distribution, and three layers for signal routing.

Two layers are dedicated solely to analog ground and digital ground planes. These two planes are electrically isolated. At the time of its design, it was unclear as to how the system grounding scheme would be implemented, so the FMC 4DAC grounds are electrically isolated. However, both ground planes can be shorted together using jumpers.

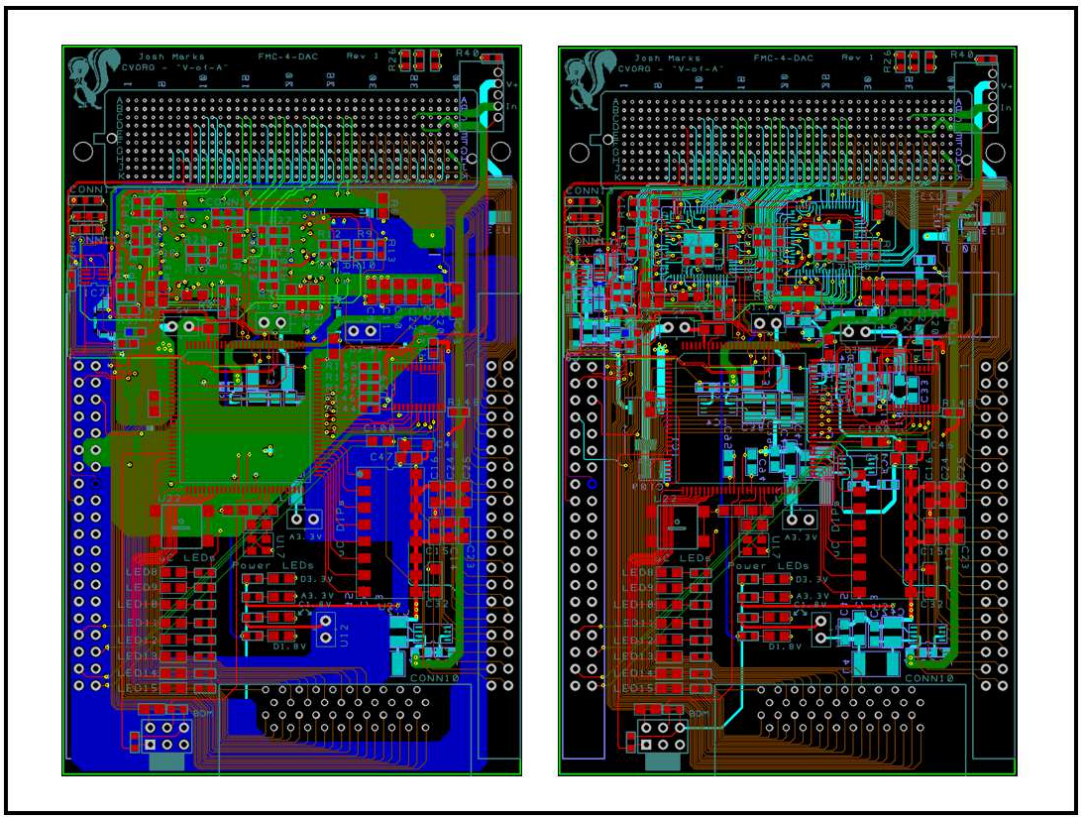


Figure 4.3 Rev 1 of FMC 4DAC with ground planes removed (left), ground planes and power planes removed (right).

The circuitry and layout for the AD9747 was designed using its datasheet as well as the schematic for the AD9747 Evaluation board. Based on the circuit schematic from the DAC Eval board we used a separate low dropout (LDO) regulator for each of the four voltage inputs to the DACs. All four LDO's are connected to a 3.3V rail provided by the FPGA over the FMC connector and grounded to the digital ground plane. The LDO's provide a high accuracy output voltage with current limiting, thermal overload protection, and a shutdown feature [23]. At the output of each LDO is a simple LC pi filter to help eliminate as much noise from the power rails as possible.

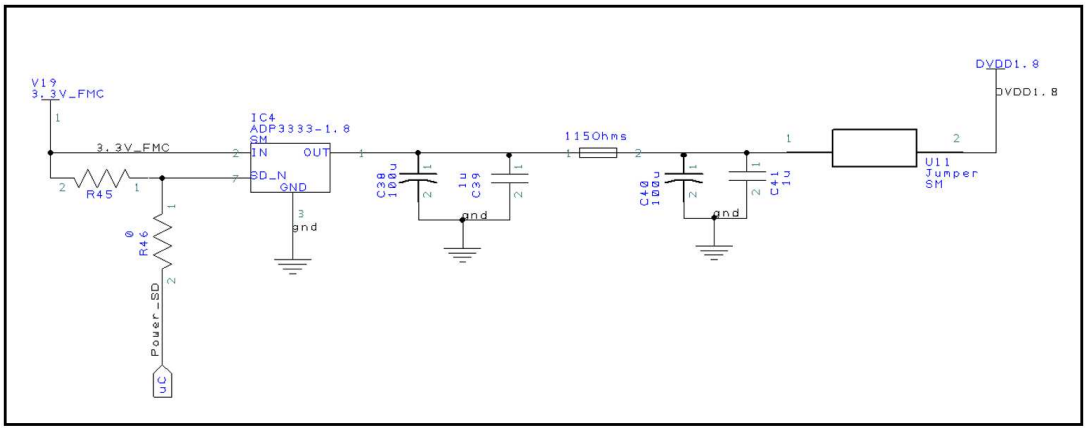


Figure 4.4 Schematic of LDO for DAC digital 1.8V

The DACs are positioned as close as possible to the FMC connector to reduce signal trace lengths. Digital address signals from the FMC connector are routed to the DACs using 5 mil traces with 5 mil spacing; the minimum trace width/spacing offered by Advanced Circuits' fabrication process. We had to use the minimum trace width and spacing in order to fit two signals between the very narrow 25 mil gaps in the pins

on the FMC connector. Figures 4.5 and 4.6 illustrate the signal routing from the FMC connector to the DACs and the spacing used.

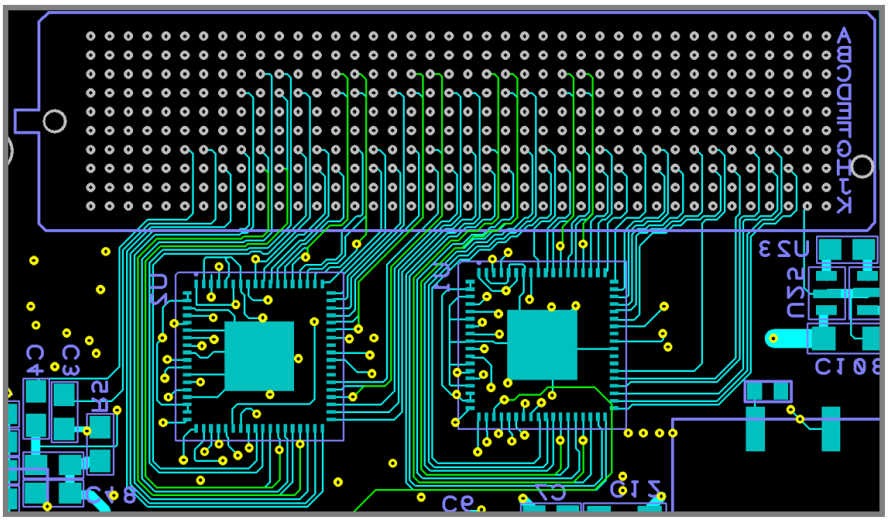


Figure 4.5 Signal routing between FMC and DACs

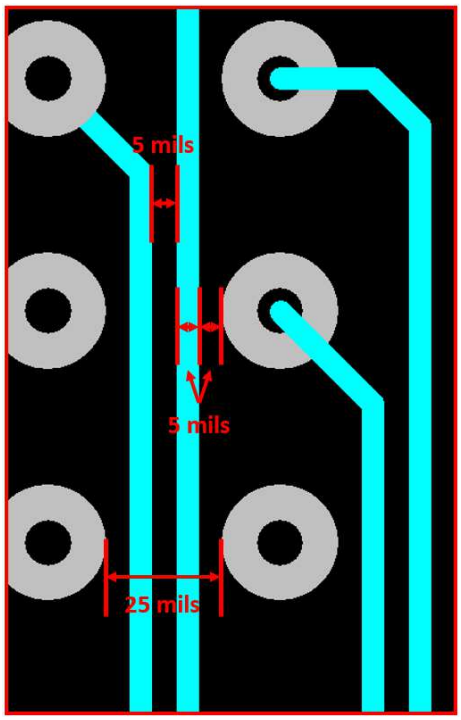


Figure 4.6 Trace spacing between FMC pins

Power for the microcontroller and analog-to-digital converter is derived from a 12V rail on the FPGA sent across the FMC connector. Before being routed to the components the 12V is converted to 6V using a DC/DC converter with high power conversion efficiency, low ripple current, and low noise. An LDO is then used to convert the 6V to 3.3V for use by the microcontroller and ADC. The 3.3V rail for the microcontroller and ADC, as well as all the power rails for the DACs, are connected to individual LEDs to indicate to the User if all power supplies are operating correctly. A bank of LEDs are also connected to GPIO pins on the microcontroller for use as status or troubleshooting purposes. GPIO pins are also connected to a push button and a dip switch bank. Special purpose pins controlled by the SPI registers of the

microcontroller are connected to the SPI pins of the DACs for initializing the DACs internal registers. Both DACs share the same master-in-slave-out (MISO), master-out-slave-in (MOSI), and SPI clock (SCLK) signals from the microcontroller. In order to allow the User to address each DAC independently each DAC is suppled with its own chip select (CS) signal. All of the SPI signals, in addition to the analog outputs from the DACs, are routed to a breakout connector at one end of the board. A separate probe board can be plugged into this connector allowing the signals to be easily probed and observed on an oscilloscope.

4.2.2 Version 2.0

A second revision of the FMC 4DAC board was needed to address some problems with the first design (discussed in Chapter 5) as well as to address changes in the overall system design. What we ended up with was a more stream lined, six layer board of the same dimensions.

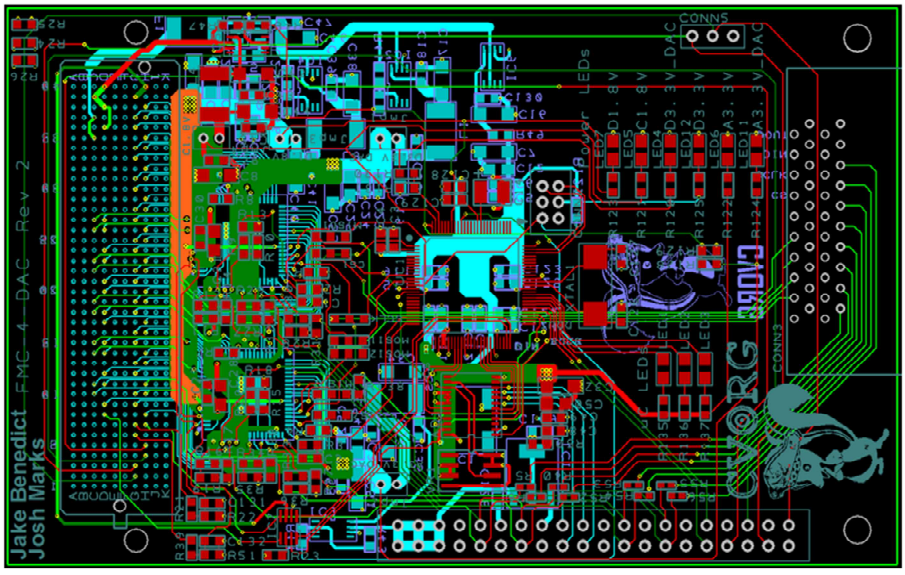


Figure 4.7 FMC 4DAC Rev 2 with ground planes removed

Revision 2 still has separate ground planes, and independent LDOs for the power supplies, but more care was taken in keeping analog and digital power separate from one another. Instead of powering all the DAC input voltages from the 3.3V rail on the FMC connector they are split them up. The digital 1.8V and 3.3V supplies for the DACs are supplied by the 12V rail. The 12V rail also supplies the LDO that creates the 3.3V digital rail for the microcontroller and ADC's digital supplies. We wanted to keep the DAC clock supply voltage as noiseless as possible to prevent noise from being coupled into the DAC's clock circuitry. A noisy clock circuit will have a degrading effect on the DAC's analog outputs, thereby reducing its performance. With this in mind, the LDO for the clock supply voltage is the only device connected to the 3.3V rail on the FMC connector. Because the digital ground from the FPGA is the ground return for the power supplies connected to the FMC connector we did not want to use the FPGA power supplies for the DAC, microcontroller, and ADC analog voltages. A 4V analog rail for the FMC 4DAC board is fed down from the Interface board, through the DAC Amp board. The 4V supply is converted into a 3.3V analog rails for the DAC, microcontroller and ADC using two separate LDOs. These LDOs are grounded to the analog ground plane, which is separate from the FPGA's ground and has a return path back to the Interface board. In Rev 1, all of the ground pins of the DACs are connected to the analog ground plane regardless of whether they are for a digital supply or analog supply. Rev 2 of the FMC 4DAC has digital supply ground pins connected to the digital ground plane and the analog ground pins connected to the analog ground plane.

During assembly of the Rev 1 boards, it was realized that the layout of the DACs has issues. Vias under the DAC chips are not covered by solder mask leaving

them exposed. Also, under-chip vias are too close to some pins and the heatsink pad of the DAC. During the solder reflow process vias are often shorted to unassociated pins or to the heatsink pad causing improper circuit behavior and component damage. To fix the issues solder mask was added to cover the vias, preventing any shorting of vias to surrounding pads. The DAC pin pads in Rev 2 are also lengthened and widened to make solder reflow and hand soldering of the DACs easier. Anticipating future system design changes, analog outputs from the DACs were rerouted to the connector feeding the DAC Amp as differential pairs instead of as single ended signals. Until the DAC Amp is changed to be a differential amplifier the negative signal of each differential pair are terminated through 50 ohm loads on the DAC Amp board.

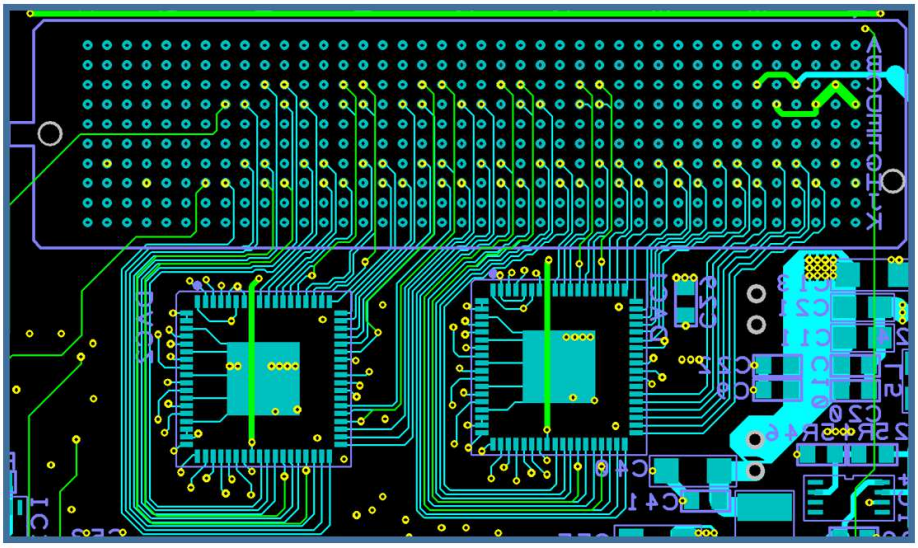


Figure 4.8 Revised signal routing and under-chip vias for Rev 2

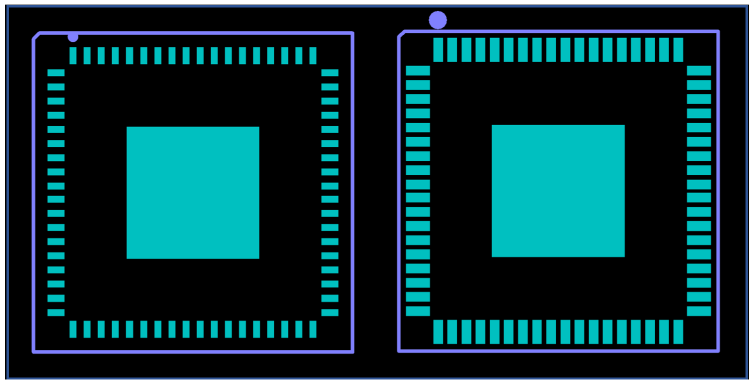


Figure 4.9 Rev 1 DAC footprint (left) vs. Rev 2 footprint (right)

For Rev 2 of the FMC 4DAC a switch from the MC9S12XET256MAL from Freescale Semiconductor to a PIC24HJ256GP210A from Microchip Technology was made. The switch to the PIC was made because the Interface board uses a PIC, which has similar features and resources as the MC9S12, but has a smaller package size. Using the same microcontroller allows code developed for one board to be used on the other. Dip switches, push button, and five of the eight status LEDs were removed because they were found to be unnecessary.

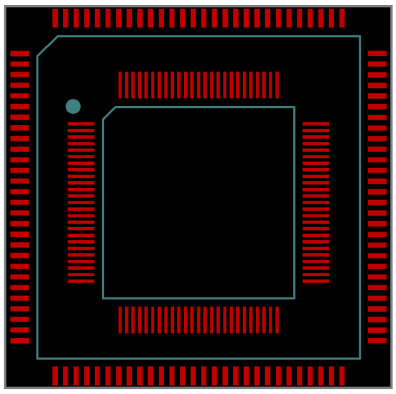


Figure 4.10 Rev 1 microcontroller footprint (outer) compared to Rev 2 microcontroller footprint (inner)

4.2.3 Version 3.0

The need for a third revision of the FMC 4DAC board was spawned by issues with the FMC connector during the assembly process. After assembly the FMC connectors have very weak connections to their pads. Testing of the Rev 2 boards revealed most of the FMC pins did not make a solid connection to their respecting pads on the board. We discovered the vias on each pad of the FMC footprint wick solder down into the vias rather then up to the pins of the FMC connector. Revision 3 addresses this problem by eliminating all on-pad vias. The vias are now located between the pads and are covered in solder mask to prevent any shorts between adjacent pins and vias. To aid in the assembly process, the Rev 3 design is tiled into 2x2 panels (four boards per panel) with global and panel fiducials. As of the writing of this thesis the Rev 3 of the FMC 4DAC has been fabricated but has not yet been assembled and tested.

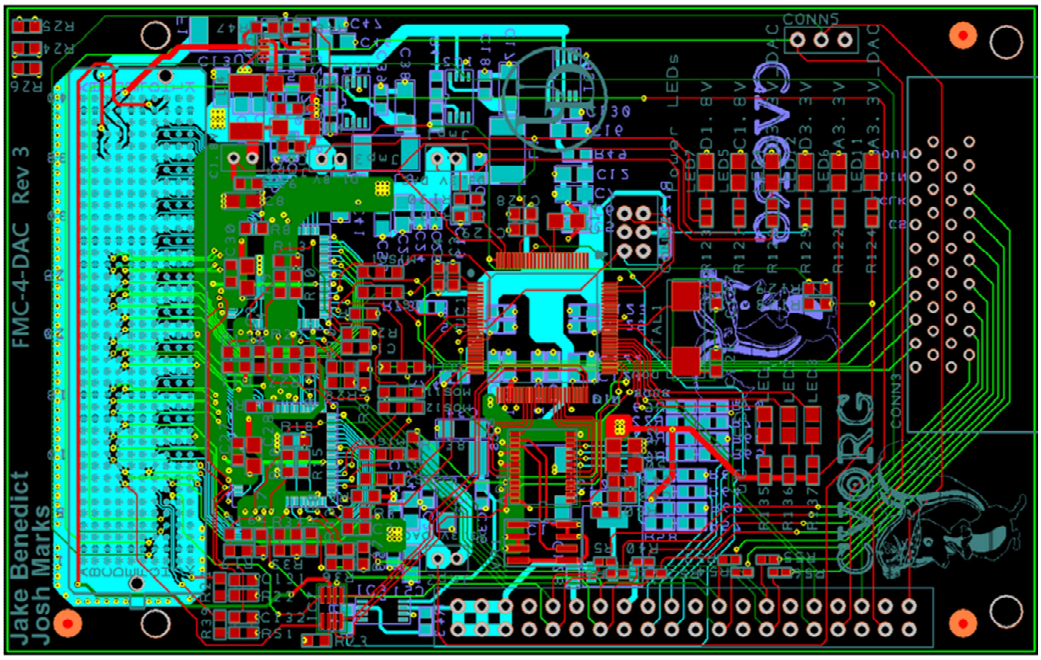


Figure 4.11 Revision 3 of FMC 4DAC

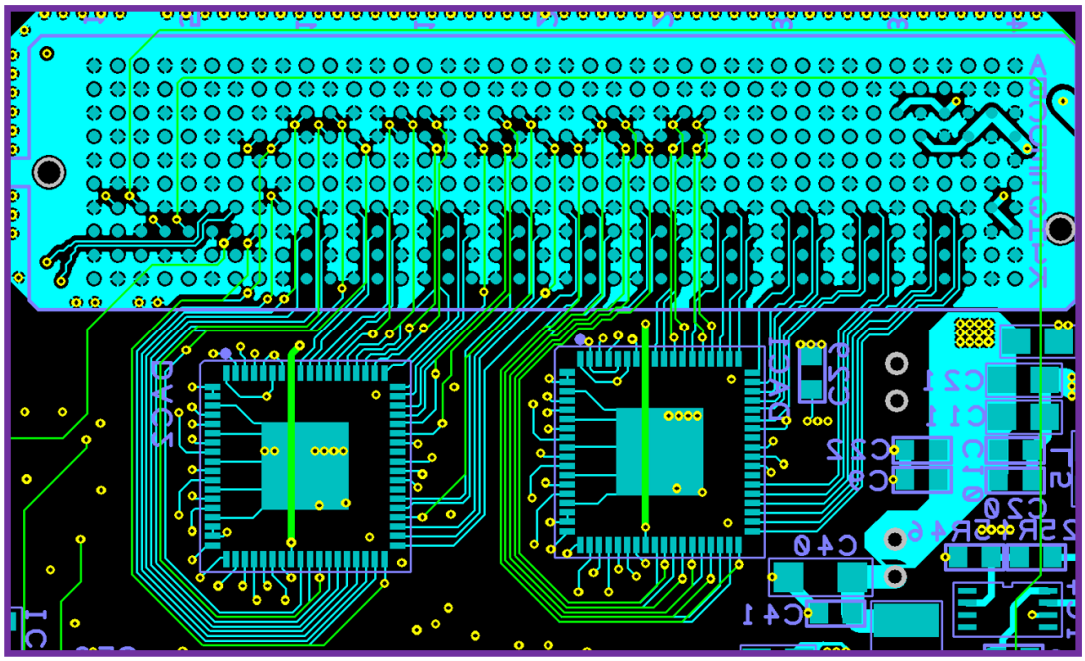


Figure 4.12 Rerouting of FMC signals for off-pad vias

Chapter 5

TEST RESULTS

At the time of testing, no FMC 4DAC Rev 2 boards had been successfully assembled due to connectivity issues between the board and FMC connector. Rev 3 boards had been fabricated, but were not back from assembly. All test results were obtained using the Rev 1 FMC 4DAC board instead. Testing of the FMC 4DAC board was performed with the board plugged into the TB-6V-LX760-LSI FPGA. Measurements were taken using a Tektronix MSO 4034B mixed signal oscilloscope with a 350MHz bandwidth.

5.1 Standalone Operation

In order to systematically test and verify the operation of the FMC 4DAC board, signal inputs and power supplies were supplied by the FPGA, while the DAC analog outputs were left unconnected to the DAC Amp board. The oscilloscope's high resolution mode was used during testing to reduce noise and increase bits of resolution in our measured signals.

5.1.1 Linearity

To accurately measure the linearity of the DACs requires highly sensitive and expensive equipment. The DACs have 16-bit resolution and output 31.7mA full scale. When using a 50 ohm load the LSB step size would be 24.2µV [see Appendix A for calculations]. This resolution is far below the 8-bit (11-bit when in Hi Res mode) resolution of our Tektronix scope [24]. Therefore, a basic observation of linearity was conducted to verify our circuit was achieving the expected performance.

The AD9747 is a current output DAC, so the voltage across an appropriate load was measured to calculate the current output. According to the datasheet, a 50 ohm load is required to achieve the compliance for the DAC voltage output. A 49.9 ohm, 1% tolerance resistor was used to load the output of the DAC and the voltage across the resistor was measured using the oscilloscope. Step sizes were increased from 1 to 6553 due to the issues with scope resolution and to reduce the amount of data points taken. Below is a graph of the digital input to DAC compared to DAC output current.

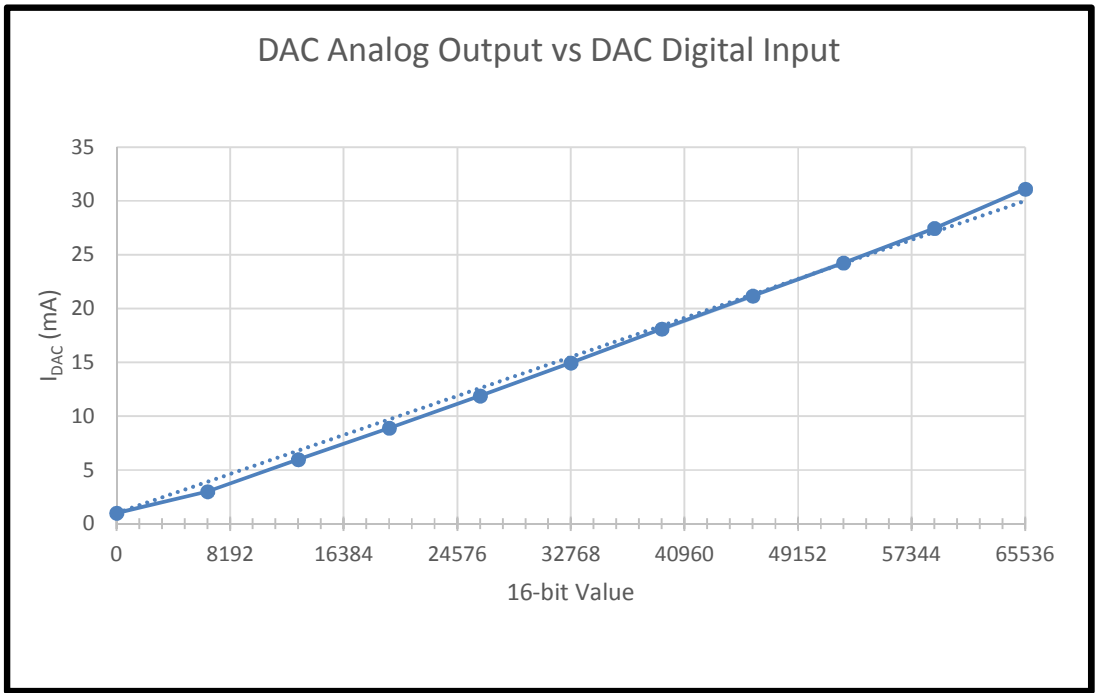


Figure 5.1 Measured DAC output current versus digital input value

From Figure 5.1 it is evident that there is some non-linearity in the DAC analog outputs, particularly at the low digital values. Some of the error in linearity at the low digital values is probably a result of higher signal-to-noise ratio when measuring the low voltage output signals. For example, when measuring the current output at a digital value of zero the scope reads a fluctuating voltage from 0V to 100mV. It is unclear as to how much of this voltage is due to noise inherent in the scope, probe, and surrounding environment, and how much is the true output of the DAC. What is clear from Figure 5.1 is that the DACs output a full scale current of 31.1mA, which is only a 1.89% gain error and within the 2% typical gain error listed in the datasheet. The equations and values used to generate Figure 5.1 can be found in Appendix A. In the future, the use of a higher resolution scope and an automated process will allow us to collect more data points more accurately to obtain a better linearity curve.

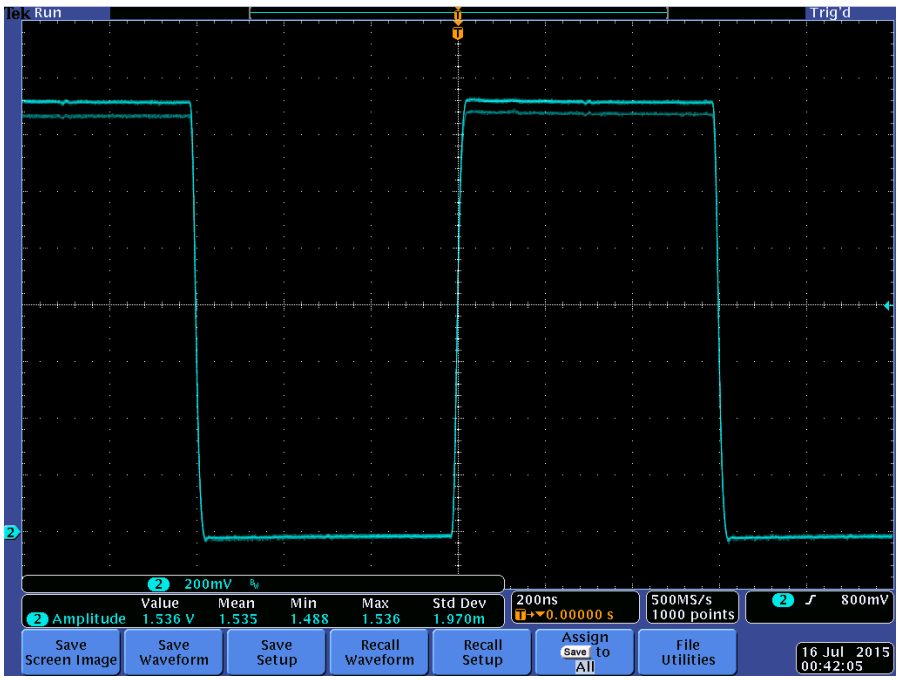


Figure 5.2 DAC output at full scale (100Hz)

5.1.2 DAC clock and signal noise

Noise on the DAC clock inputs can couple onto the DAC analog outputs degrading system performance. Measurements were taken of the differential clock provided by the FPGA to observe clock performance.

Figure 5.3 Positive DAC clock supply from FPGA before voltage division (yellow) and after clock voltage division (blue) at 1.67MHz (100Hz frame refresh rate)

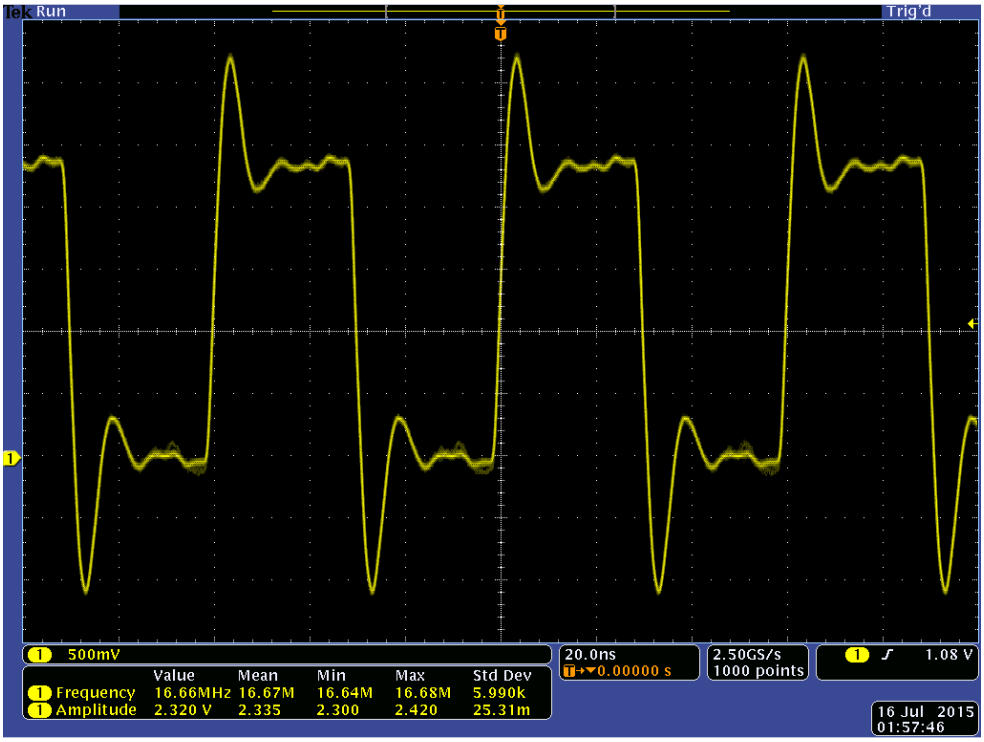


Figure 5.4 DAC positive clock input before voltage division at 16.67MHz (1kHz frame refresh rate)

Running the DACs to simulate a system 100Hz frame refresh rate produced the 1.67MHz clock in Figure 5.3. Some over shoot and undershoot is evident at the rising and falling edges of the clock pulses, but these small fluctuations are tolerable at the 100Hz speed. The rising time is 2ns with a settling time of 80ns. When the DAC clock frequency is increased to 16.67MHz, achieving a 1 kHz frame refresh rate, the clock signal degrades significantly. It can be seen from Figure 5.4 that the overshoot and undershoot become more pronounced and the settling time takes up the full 30nS peak/trough hold time. In addition, the clock rise time doubles to 4ns. The same noise degradation of the clock signal is measured when the FMC 4DAC board is removed and the signal is probed directly off the FPGA FMC connector. Little can be done to

address the signal quality coming from the FPGA, however Rev 3 of the FMC 4DAC board has capacitors in its clock voltage divider networks that may prove to dampen some of the over/undershoot. The DAC clock can run on a sinewave clock signal, so shaping the clock to more resemble a sinewave is acceptable.

Further observations were made to examine if ringing on the clock lines was contributing any noise to the DAC digital input data and analog output signals.

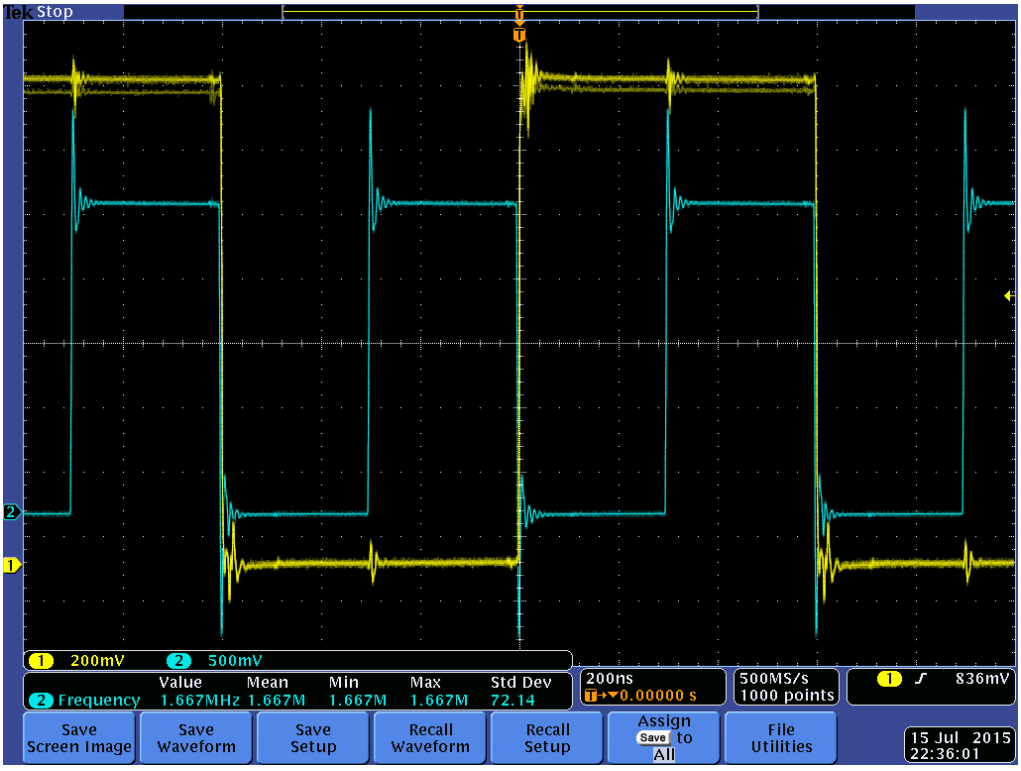


Figure 5.5 DAC output (yellow) with noise from DAC clock (blue) at 100Hz frame rate

In Figure 5.5 the switching noise from the clock can be seen on the analog output from the DAC. At 100Hz the noise contribution from the clock is minimal and has no discernible negative effects on system performance.

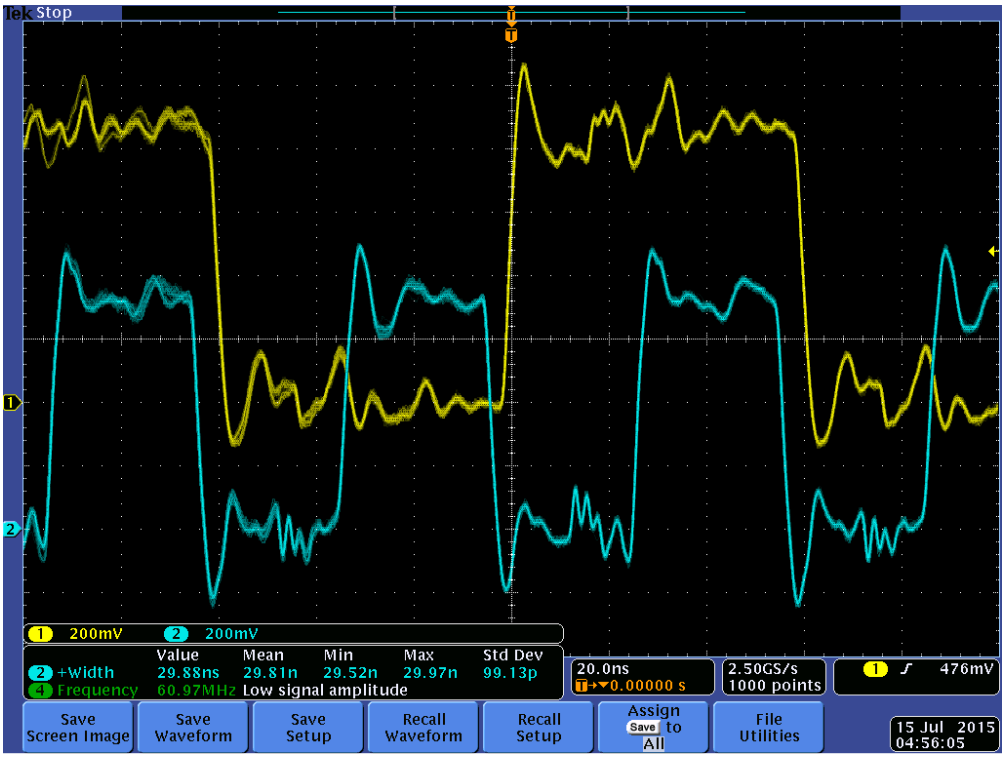


Figure 5.6 DAC current out (yellow) and DAC clock (blue) at 1kHz frame rate

Figure 5.7 DAC input data (yellow) and DAC clock (blue) at 1kHz frame rate

Increasing to a 1 kHz frame rate, the noise from the clock signal begins to dominate the DAC analog outputs, as can be seen in Figure 5.6. Using the analog outputs at 1 kHz proves difficult since the noise on the analog lines degrades the performance of the amplifiers on the DAC Amp board. The next section discusses the performance of the DACs when loaded with the amplifiers and the rest of the TCSA system. Looking at the waveforms in Figure 5.7 the digital input signal looks very similar to the clock waveform. This similarity has little to do with noise interference between the two, but is a result of both signals being generated by the same source on the FPGA. This relationship suggests that perhaps the noise is from the FPGA's ground plane or power supplies. Future efforts will be made to investigate the cause of

the noise on the clock and data signal and if there are any solutions that can be implemented.

5.2 In-system Testing

To characterize the performance of the FMC 4DAC when fully integrated into the TCSA system the DAC outputs were observed when connected to the DAC Amp and Interface board. Probes were placed on the inputs and outputs to the amplifiers on the DAC Amp board. The DACs were set to operate at full scale and measurements were taken at 100Hz, 400Hz and 1 kHz frame rates. Waveforms observed at the different frame rates are shown in the figures below.

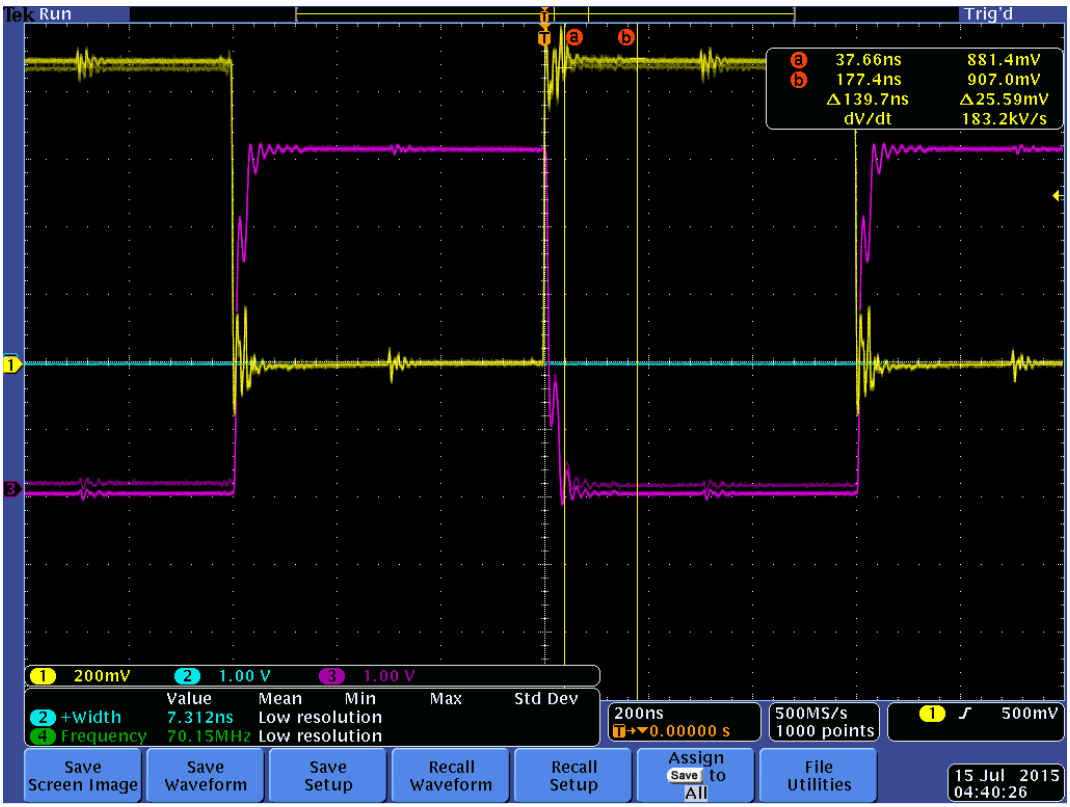


Figure 5.8 DAC output (yellow) and amplifier output (pink) at 100Hz

Figure 5.9 DAC output (yellow) and amplifier output (pink) at 400Hz

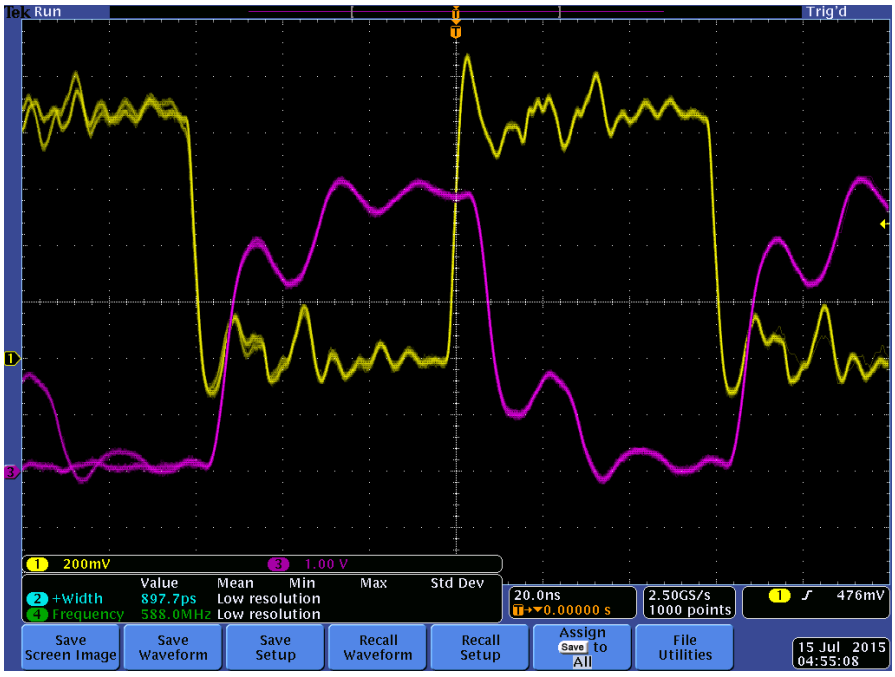


Figure 5.10 DAC output (yellow) and amplifier output (pink) at 1kHz

Figures 5.8 – 5.10 illustrate the degradation of the analog signals as the frequency of the system frame rate is increased. Frame rates between 100Hz and 400Hz appear to produce usable analog signals, but may not provide full 16-bit accuracy. Frame rates approaching 1 kHz yield analog signals that are unacceptable for system performance. Comparing the DAC analog outputs when driving a 50 ohm load and when driving the amplifiers, it can be seen that more noise exists on the analog lines when the FMC 4DAC is integrated into the system. Since the noise contribution from the oscilloscope and probes remains the same through both tests, the sources of the noise lie somewhere in the interaction between the amplifiers and the DACs. One source of the noise stems from the poor ground and power separation of analog and digital signals on the Rev 1 board. Future testing will determine if the improved isolation of analog and digital signals on the Rev 3 FMC 4DAC improves signal integrity. Plans for the future also include utilizing the differential output of the DAC channels, which may have a positive impact on improving signal integrity.

Chapter 6

CONCLUSION

As a first attempt, the first revision of the FMC 4DAC board has proven useful for preliminary system testing. System development has been able to move forward with the use of the Rev 1 board and it has logged over a hundred hours of operation time. Moreover, it has successfully demonstrated improved system frame rates of up to 400Hz. While these milestones are promising, Revision 1 of the FMC 4DAC does fall short of the 1 kHz frame rate objective of the TCSA project. In addition, only one board has ever been successfully assembled due to the incorrect layout of the FMC connector causing connectivity issues as mentioned in section 4.2.3. Scalability is an important goal for the TCSA system and it cannot be met using the Rev 1 FMC 4DAC board. In order for the FMC 4DAC to be considered a fully usable component of the TCSA CSE improvements are needed in signal integrity and the ability to produce multiple units quickly must be achieved.

Many of the issues facing the first revision of the FMC 4DAC have been addressed in the third revision. The complete isolation of the analog and digital grounds and power rails on Rev 3 of the board is expected to eliminate noisy ground loops and reduce coupling between analog and digital signals. The noise injected into the analog outputs from the DAC clock, as observed in section 5.1.2, is addressed, and hopefully eliminated, in the latest revision with dampening capacitors in the clock voltage divider network for smoothing the over/undershoot seen on the clock edges. Scalability of Rev 3 has yet to be seen, but with the changes made to the FMC

connector layout a successful assembly of multiple units is expected in the very near future.

The design and layout of mixed signal, analog/digital PCBs is a very complex and often difficult endeavor. Through the different iterations of the FMC 4DAC board a lot of knowledge and experienced was gained, and many lessons were learned in analog/digital design. It is my hope that the experiences outlined in this thesis will provide a base from which new ideas and understanding can spawn as the TCSA project continues to progress and mature.

REFERENCES

1. C. Lange, “Design and development of a 512x512 infrared emitter array system,” *Master’s Thesis*, University of Delaware, Department of Electrical and Computer Engineering, June 2011.

2. R. McGee, F. Kiamilev, N. Waite, J. Marks, K. Nabha, G. Ejzak, J. Dickason, J. Benedict, M. Hernandez, “512x512, 100Hz mid-wave infrared LED scene projector,” *2015 GOMAC*, St. Louis, Missouri. (March 2015)

3. P. Bryant, J. Oleson, J. James, B. Lindberg, J. Lannon, D. Vellenga, S. Goodwin, A. Huffman, C. Pace, S.L. Solomon, “MIRAGE: developments in IRSP system development, RIIC design, emitter fabrication, and performance,” *Proc. SPIE*, vol. 5408, p. 173, Aug. 2004.

4. J. James, P. Bryant, S. Solomon, J. LaVeigne, G. Matis, J. Oleson, J. Lannon, S. Goodwin, A. Huffman, “OASIS: cryogenically-optimized resistive arrays and IRSP subsystems for space-background IR simulation,” *Proc. SPIE*, vol. 6208, p. 620812, May 2006.

5. P.T. Bryant, J. Oleson, B. Lindberg, K. Sparkman, S.W. McHugh, S.L. Solomon, “1024x1024 large format resistive array (LFRA) design, fabrication, and system development status,” *Proc. SPIE*, vol. 5092, p. 91, Sept. 2003.

6. K. Sparkman, J. LaVeigne, S. McHugh, J. Kulick, J. Lannon, S. Goodwin, “Scalable emitter array development for infrared scene projector systems,” *Proc. SPIE*, vol. 9071, p. 90711, May 2014.

7. V.K. Malyutenko, K.V Michailovskaya, O.Yu. Malyutenko, V.V. Bogatyrenko, and D.R. Snyder, “Infrared dynamic scene simulating device based on light down-conversion,” *IEE Proc.-Optoelectronics*, vol. 150, no. 4, Aug. 2003.

8. E.J. Koerperick, D.T. Norton, J.T. Olesberg, B.V. Olson, J.P. Prineas, and T.F. Boggess, “Cascaded superlattice InAs/GaSb light-emitting diodes for operation in the long-wave infrared,” *IEEE Journal Quantum Electronics*, vol. 47, no. 1, pp. 50-54, Jan. 2011.

9. K. Nabha, “100 Hz 512x512 SLEDS system design,” *Master’s Thesis*, University of Delaware, Department of Electrical and Computer Engineering, June 2014.

10. J. Marks, F. Kiamilev, N. Waite, R. McGee, “Read-in integrated circuits for large-format multi-chip emitter arrays,” *2015 GOMAC*, St. Louis, Missouri. (March 2015)

11. L.M. Murray, “Investigations into molecular beam epitaxial growth of InAs/GaSb superlattices,” *Doctoral Dissertation*, University of Iowa, 2012.

12. T.F. Boggess, J.L Hicks, E.J. Koerperick, J.T. Olesberg, J.P Prineas, “Active region cascading for improved performance in InAs/GaSb superlattice LEDs,” *IEEE Journal of Quantum Electronics*, vol. 44, no. 12, Dec. 2008.

13. C. Cole, “Real digital, a hands-on approach to digital design,” *Xidian University Press*, pp. 36, 2009.

14. C. Kerwien, “Design and characterization of 12V analog trans-impedance amplifier for superlattice LED projector,” *Honors Bachelors Thesis*, University of Delaware, Department of Electrical and Computer Engineering, June 2013.

15. R. Rehrig, “Design and development of a 2-color infrared emitter array system,” *Master’s Thesis*, University of Delaware, Department of Electrical and Computer Engineering, June 2012.

16. T. Boggess, “Two color SLEDS array (TCSA),” PowerPoint slides, EWT Phase 1 Decision Meeting, Jan. 2014.

17. XILINX, “Virtex-6 family overview,” Product specifications, Jan. 2012.

18. Inrevium, “Tb-6v-lx760-lsi hardware user manual,” User manual, July 2012.

19. G. Ejzak, J. Dickason, R. McGee, K. Nabha, J. Marks, J, Benedict, N. Waite, M. Hernandez, H. Ahmed, S. Cockerill, F. Kiamilev, “Scalable and modular architecture for close support electronics of an infrared scene projector,” *2015 GOMAC*, St. Louis, Missouri. (March 2015)

20. Analog Devices, “Dual 8-/10-/12-/14-/16-bit 250 MSPS digital-to-analog converters,” AD974x datasheet.

21. R. Seelam, “I/O design flexibility with the FPGA mezzanine card (FMC),” www.vita.com, Aug. 2009, Xilinx. July 2 2015 <http://www.vita.com/Resources/Marketing%20Alliances/FMC/Xilinx_wp315.pdf>.

22. Molex, “Product specifications Searay connector system,” FMC datasheet, Oct. 2013.

23. Analog Devices, “High accuracy ultralow IQ, 300mA, anyCAP low dropout regulator,” ADP3333 datasheet.

24. Tektronix, “Mixed signal oscilloscope: mso4000B, dpo4000B series datasheet,” datasheet, April 2013.

Appendix A

CALCULATIONS AND TABLES FOR SECTION 5.1.1

Calculating LSB step size of AD9747:

$$\frac{full\ scale\ current\ (A)}{bits\ of\ resolution} \times load\ resistance\ (ohms) = LSB\ step\ size\ (V)$$

$$\frac{31.7mA}{16\ bits} \times 50\ ohms = 24.2\mu V$$

16-bit value	Voltage across 50 ohm load (mV)	Current output (mA)
0	0 -100	1.01
6553	144 - 152	2.99
13107	296	5.98
19660	440	8.89
26214	584 - 592	11.88
32767	736 - 744	14.95
39321	896	18.1
45874	1048	21.17
52428	1200	24.24
58981	1360	27.47
65535	1540	31.11

Table A.1 Measured and calculated values for DAC linearity

Equation for calculation of values in "Current output" column of Table A.1:

$$\frac{voltage\ across\ load\ (V)}{load\ resistance\ (ohm)} = current\ output\ (A)$$